SWITCHING STRATEGIES FOR AC/AC VECTOR SWITCHING MATRIX CONVERTERS

by

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ABSTRACT

This thesis proposes switching strategies for AC chopper converters which can implement the multiple steps switching technique and convert the AC energy to AC, directly. The switching process in this technique depends on the current direction in the load.

The main advantage of the technique is that the load will not be disconnected during switching events. Also, the semi–soft switching topology overcomes the switching problems in the AC chopper converters, without increasing the conduction losses of the devices. In addition, this topology does not require a dead–time, an attribute that is essential in the other topologies for ensuring that there is not a short circuit on the input source. In addition, during the dead–time in the traditional AC chopper, the load current is completely disconnected from the power source and drains across the snubber circuits, including increased power losses and a bulky snubber circuit.

The advocated semi–soft switching topology achieves the multiple step switching and reduces the switching losses, as compared to the hard switching topology with dead–time.

A comprehensive analysis is performed including operating principles and all calculations of the currents and power losses. Finally, computer simulations of the applications are executed to validate the approach.

This abstract accurately represents the content of the candidate's thesis. I recommend its publication.

Approved: Fernando Mancilla–David

DEDICATION

I lovingly dedicate this thesis to my hardworking family, my late father (may Allah have mercy on him and grant him Paradise, Aameen), and to my affectionate mother as well. Also, I loyally dedicate this thesis to my wife who has been a great source of motivation and inspiration.

ACKNOWLEDGMENT

All praises to the Sustainer of the worlds, and grace, honour and salutations on the Chief of Apostles and Seal of Prophets, Mohamed, his family, companions and those who followed him in an excellent fashion and invited mankind towards Allah, until the Day of Resurrection.

I'm truly grateful to Allah, for giving me the strength and patience to complete this work. I would also like to thank Allah for giving me good health throughout the research until I have completed this thesis.

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1. Introduction

The control of power flow in AC transmission systems is complex and is established by good management of power flow between nodes and interconnecting branches [1]. Although AC power systems have a strong connectivity, the control of power systems remained limited until the recent developments of controllers that use the power electronic devices. These controllers have greatly enhanced the capability to control AC transmission systems [2, 3]. The technique of switching power flow–control was presented by using a DC switching converter. However, more recently this technique was developed to three phase Vector Switching Matrix Converter (VeSMC). Vector Switching Matrix Converters have the ability to control and modulate power flow between multiple power lines in a complex system [16]. The matrix converters have attracted great attention recently. Moreover, compared to the conventional AC/DC/AC converters, the matrix converter has the following virtues [19, 20, 4]:

1. Both input current and output voltage are sinusoidal waveforms with slight harmonics around the switching frequency.

2. No large components, such as large DC smoothing capacitors or smoothing inductors, are needed for energy storage except a small size AC filter.

3. ery simple to construct and has powerful controllability.

In addition, devices based on AC link power converters have been presented in [8, 10, 11], which have a functional capability that is equivalent to DC link

devices. Theses DC link devices store twice as much energy as AC links. Therefore, they need more power semiconductor which increase the cost of the power components in the DC link power converters. On the other hand, the power semiconductors loss in the AC link is approximately 15% more [9]. Due to the relatively large physical volume of the DC link energy storage element, compared with the entire converter volume, the lifetime of the converter may be reduced [6]. An overview of the DC link converter topologies used to implement a three–phase Pulse Width Modulation (PWM) AC–AC converter system has been presented in [6]. The topology of the Indirect Matrix Converter (IMC) is developed from the DC link back–to–back by neglecting the DC link capacitor, and the three–phase AC–AC Buck–type chopper is considered as a special case of Matrix Converter (MC). In general, the three–phase AC–AC Buck converters can only control the amplitude of the output voltage to be less than or equal to the input voltage, and the control system in these converters is based on PWM with a constant duty cycle [15]. AC choppers are not designed to change the frequency. Accordingly, the fundamental output frequency will be equal to the frequency of the input source. These converters are usually used as voltage regulators and voltage sag compensators in the distribution system as well as a power flow controller in the transmission power systems. In other words, the main applications of the AC chopper are power conditioning in the distribution systems and power flow in the transmission lines. There are two applications in the power conditioning where the AC chopper can be implemented. Firstly, in the full power condition, the fixed AC voltage will be as an input of the AC chopper and the variable AC voltage will be achieved as an output from the AC

chopper which depends on the duty ratio. Secondly, in the partial power condition, the input of the AC chopper is the grid voltage and the output is connected to the grid via a series transformer. Consequently, in the series connected AC chopper, the switches rating can be reduced. In the first application as shown in Fig. 1.1 the total power of the load is flowing through the converter, resulting in large switches rating and high cost [5]. This type of AC chopper can be used to control the voltage at sensitive loads directly, as shown in Fig. 1.1. However, in other applications, the AC chopper is used in the mid–point of a transmission line with an isolation transformer as shown in Fig. 1.2 [8, 17].

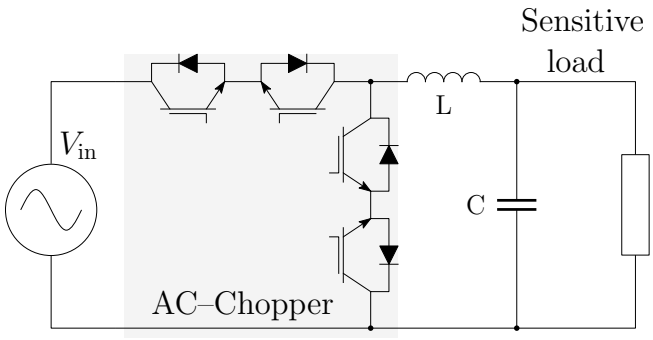


Figure 1.1: Single–phase Buck–type AC–Chopper

Furthermore, the AC chopper can be combined with a series injection transformer for power flow control in the transmission lines as it shown in Fig. 1.3. In this case, the power rating of the converter is smaller than the power rating of the load. Ultimately, the AC choppers are used where there is a need to change the magnitude of the AC voltage, such as soft starting of induction motor, speed controllers, and heating systems.

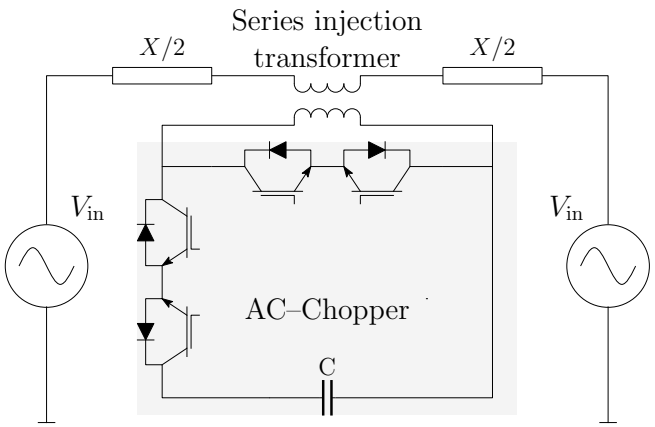


Figure 1.2: PWM AC–AC Converter

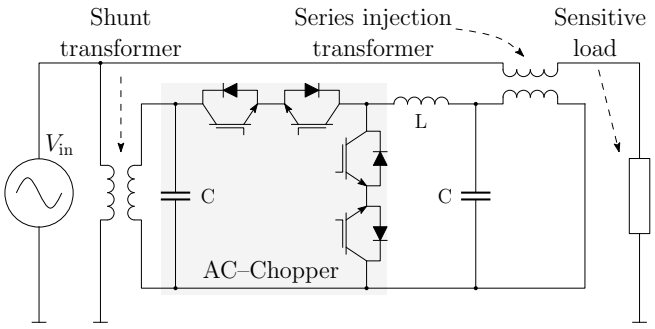


Figure 1.3: AC chopper Combined with Isolation Transformer.

Recently, the research on the applications and the topologies of the AC–AC converters has gained attention. However, very little interest has been paid to the challenges in the AC choppers switching process. Consequently, most of the offered AC choppers deploy hard switching PWM converters which, in the high power applications, induce high switching loss and low efficiency. Thus, via the use of either Zero–Voltage Switching (ZVS) for the transistors or Zero–Current Switching (ZCS) for the diodes, soft switching techniques for the converters may be deployed to obtain minimal switching loss and higher efficiency as well [13]. In addition, the soft–switching topology exhibits better efficiency than the hard–switching topology [13].

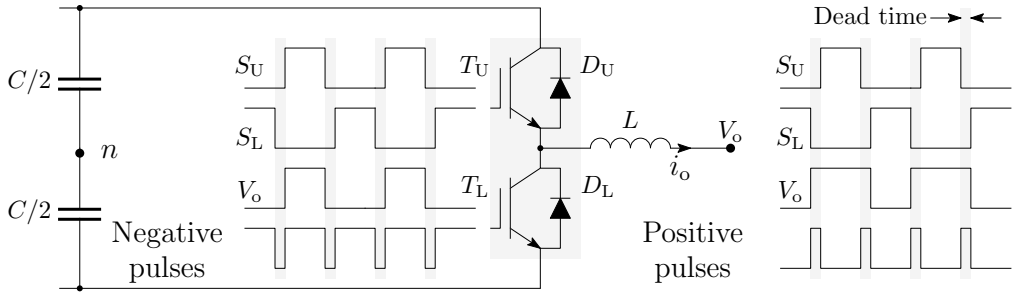


Figure 1.4: Effect of Dead–time on Output Voltage

In addition, all the hard switching topologies with dead–time increase the losses, one of the main resulting difficulties being the snubber design in the AC choppers. Fig. 1.4 shows the dead–time effect in the VSC. Assuming that the output current flows out from the phase–leg as shown in Fig. 1.4, the current flows through the upper transistor T_{U}; when the latter is on, while the lower diode D_{L} induces a free–wheeling when the upper transistor T_{U} is off. In this

situation, the direction of the draining current is positive. Thus, only the upper transistor T_{U} and the lower diode D_{L} are active, which ensures there is a path for the load current to flow. When the current flows in a negative direction, only the lower transistor T_{L} is on and freewheels through the upper diode D_{U}. Both transistors can not be on nor off simultaneously; they switch complementarily [7]. During the dead–time, both switches S_{U} and S_{L} are off. For instance, in the inductive load, the output voltage depends on the direction of the output current which is conducted during the dead–time by either the upper or the lower diode and voltage gain or loss will occur as a result. Therefore, the positive pulses and the negative pulses in Fig. 1.4 correspond to the gain and loss of the voltage, respectively [21].

A comparative evaluation of AC–AC vector switching matrix converters, in order to evaluate loss and efficiency, has been presented for different topologies feeding the same load. The semi–soft switching technique and hard switching technique have been implemented and detailed using computer–matlab simulation to prove the operation principle of each technique.

2. Multiple Steps Switching Capability

2.1 Examined Topologies

In this chapter, all the switches are considered ideal and no dead–time is taken into account in all the examined topologies.

The switching process in the topologies depends on the current direction in the load. Therefore, according to the current direction there are six different cases or operation modes; each case is 60° as it shown in Fig. 2.1.

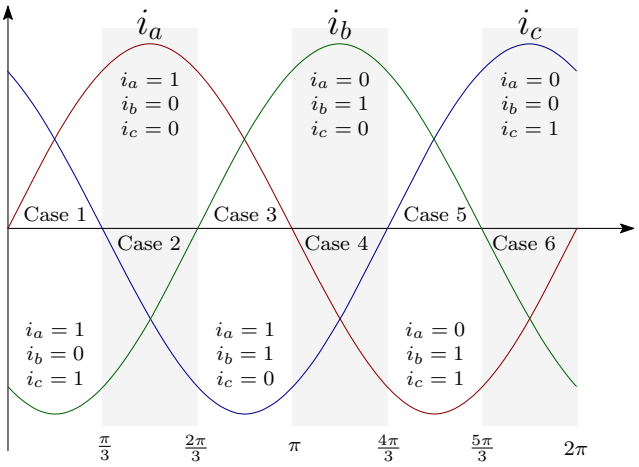


Figure 2.1: Current Direction States

So, finding the direction of the load current requires digital indicators as shown in Fig. 2.2(a), which give *zero* when the load current is negative or *one* when the load current is positive. Consequently, comparing the value of load current with zero at each phase generates the six–pulse cases as it is shown in Table 2.1

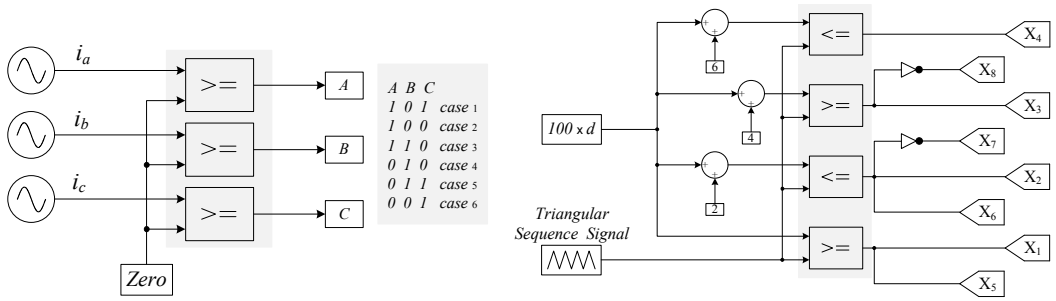
Currents	**Case 1**	**Case 2**	**Case 3**	**Case 4**	**Case 5**	**Case 6**
i_{a}	1	1	1	0	0	0
i_{b}	0	0	1	1	1	0
i_{c}	1	0	0	0	1	1

Table 2.1: Six–Pulse Cases

In general, the multiple steps switching strategy can be summarized as follows [14]:

1. Detect the direction of the current load.
2. Switch *off* the transistor that is not draining any current at present.
3. Switch *on* the transistor which will drain the load current in the same direction.
4. Switch *off* the transistor which is presently draining the load current; this will make a new path for the current.
5. Switch *on* the other transistors in the active switch.

When the current is *zero*, it is not important if the output signal is *zero* or *one*. Therefore, the current can be considered as a negative current or a positive current in the switching process ($I_{\mathrm{a}} = 1$ is positive and $I_{\mathrm{a}} = 0$ is negative). This chapter describes the topologies and the switching strategies for each.



(a) Current Direction Signals (b) Control Signals for Multiple Steps Switching

Figure 2.2: Generated Signals

2.2 First Topology with 6 Switches and 6 Diodes

The first topology is shown in Fig. 2.3 with two three–phase switches using the multiple steps switched Buck–type AC chopper half of the time. Turning the switches *on* and *off* in this topology needs eight control signals that are shown in Fig. 2.2(b). This topology implements the multiple steps switching technique in a half power period of time and a hard switching technique for the other half power period. In other words, it is not possible to do soft switching for all switches during the entire power period.

Note that the two three–phase switches can not be closed at the same time in this topology because this causes a short circuit on the three phase voltage source. Similarly, both three–phase switches can not be open at the same time in this topology because the load will be disconnected and remain in an open circuit, which may generate voltage spikes [4]. In the case of doing hard switching, one of the three–phase switches should be closed while the other switch is open

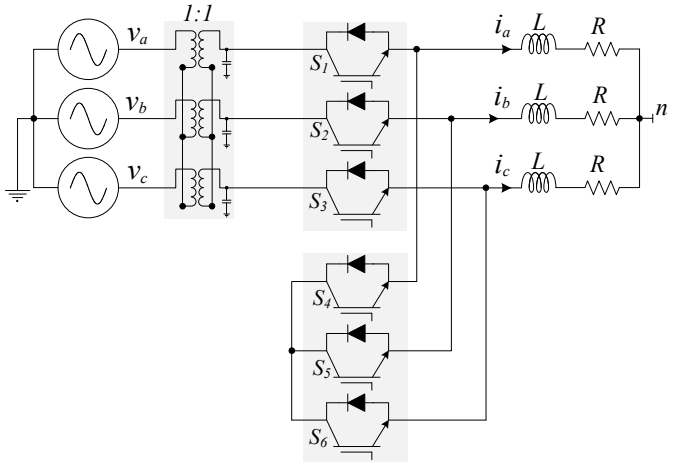


Figure 2.3: First Topology

and vice versa. However, the switching technique in this topology is applied by the following two procedures:

1. The cases 1, 3 and 5 in Fig. 2.1 use the signals X_5, X_6, X_7 and X_8, which are shown in Fig. 2.2(b) to control the two switches that drain the current at the same time and the hard switching technique can be achieved through the following procedure:

   (a) Switch *off* the transistor that is not draining any current in the active three–phase switch.

   (b) Switch *on* the two transistors which will be finally draining the current in the non–active three–phase switch and switch *off* the two transistors that are draining the current in the active three–phase switch at the same time (this is a hard switching).

   (c) Switch *on* the other switch in the three–phase switch that is finally

draining the current.

Precisely, this procedure is implemented when the current is positive in two phases and negative in the other phase. For example, when the current in both phases A and C is positive and negative in phase B (this is *case* 1) as shown in Fig. 2.4.

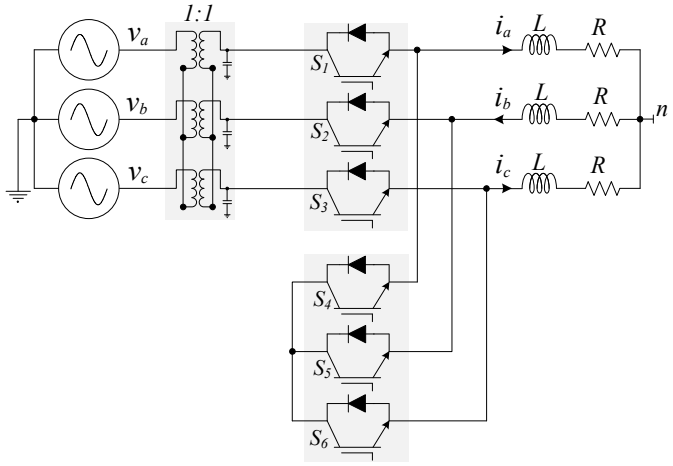


Figure 2.4: Case 1, i_{a} and i_{c} are Positive, i_{b} is Negative

Fig. 2.5 shows the switching process for *case* 1 when the current in phases A and C is positive and is negative in phase B. In this case, the load is connected to the input voltage source with the switches S_1, S_2 & S_3 while the other switches are *off*. Following the first procedure mentioned above, the transistor that is not draining any current is S_2. Thus, Fig. 2.5(b) shows the direction of the currents after switching off S_2 which remained constant and flowing through S_1 & S_3 keeping the load connected to the voltage source. In *state* 3, after switching on S_4 & S_6 simultaneously with

switching off S_1 & S_3 (this is a hard switching), the input voltage source will be disconnected and the load will be shorted in a new path through S_4, S_5 & S_6 to keep the load currents flowing in the same directions as can be seen in Fig. 2.5(c). Finally, switch on S_5 in Fig. 2.5(d) which is not draining any current in this case. It is important to mention that the switching technique in this case is only hard switching. However, the soft switching will be applied in the next case by following the second procedure:

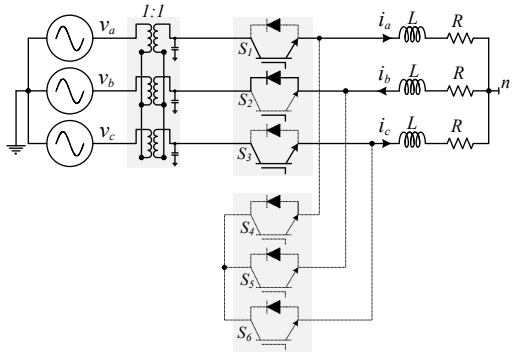
2. In the cases 2, 4 and 6 in Fig. 2.1, there is only one transistor that drains a positive current all the time and the other two negative currents will be flowing through the diodes. So, according to the current direction in the load, these cases use the signals X_1, X_2, X_3 and X_4, which are shown in Fig. 2.2(b) to control the switches and to implement the multiple steps switching technique by following the next procedure:

   (a) Switch *off* the two transistors that are not draining any current in the two phases that have a negative current in the active three–phase switch.

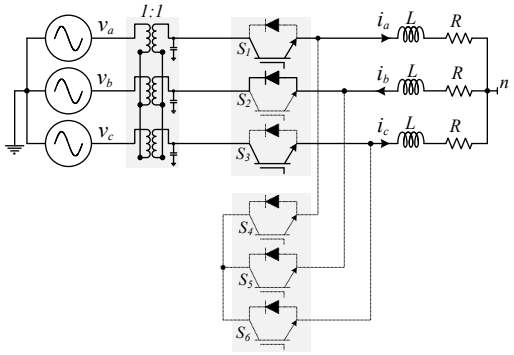
   (b) Switch *on* the transistor that will be draining the positive current in the other phase in the non–active three–phase switch.

   (c) Switch *off* the transistor that is draining the positive current in the active three–phase switch so the other three–phase switch will be activated as a result.

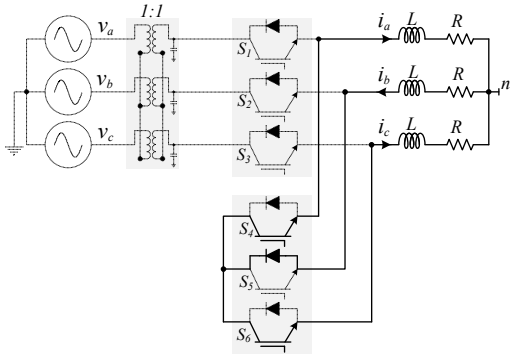
   (d) Switch *on* the other two transistors in the active three–phase switch.



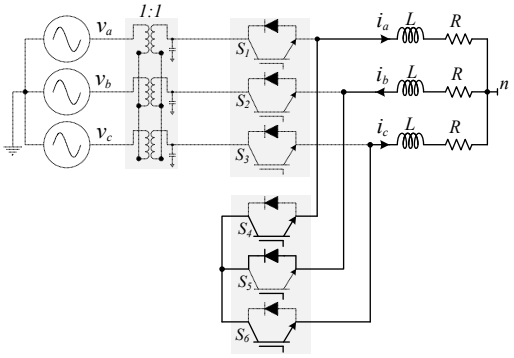
(a) State 1, S_1 &S_3 are draining a positive current



(b) State 2, turn–off S_2 while the currents are still flowing through S_1 &S_3



(c) State 3, S_4 &S_6 are draining a positive current



(d) State 4, turn–on S_5 which is not draining any current

Figure 2.5: Switching Process during Case 1

Previous cases occur when the current is negative in two phases and is positive in the other phase. For example, case 2 is when the current in phases B and C is negative, and the current in phase A is negative, Fig. 2.6.

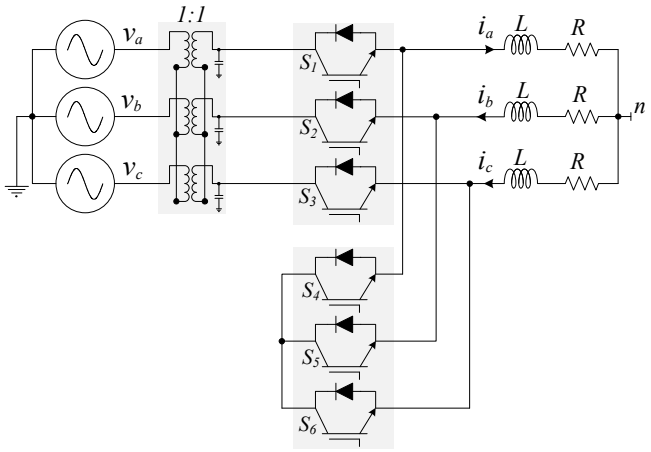


Figure 2.6: Case 2, i_{b} and i_{c} are Negative , i_{a} is Positive

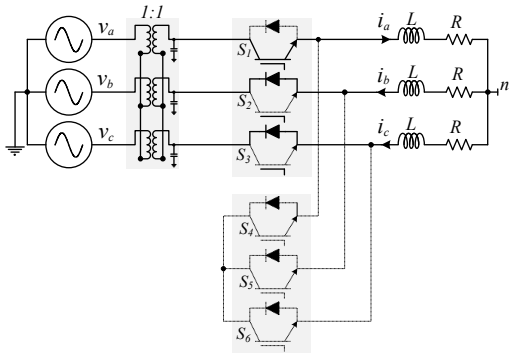
Fig. 2.7 shows the switching process for *case* 2 when the current in the phases B and C is negative and the current in the phase A is positive. In this case, the load is connected to the input voltage source with the switches S_1, S_2 & S_3 while the other switches are *off*. Following the second procedure mentioned above, the two transistors that are not draining any current in this case are S_2 & S_3. Therefore, *State* 1 in Fig. 2.7(a) shows the load connected to the input voltage source with the switches S_1, S_2 & S_3 while the other switches are *off* and as it can be seen, in the same figure, the transistors in the switches S_2 & S_3 are not draining any current. However, in *State* 2 Fig. 2.7(b) after switching *off* (S_2 & S_3), S_1 is the only transistor that drains current. To keep the current flowing in the same direction, it should switch *on* S_4 before disconnecting the

input voltage source from the load as in *State* 3 Fig. 2.7(c). In *State* 4, Fig. 2.7(d) switching *off* the transistor that is draining the positive current which is S_1, will immediately change the current path and keep the currents flowing in the same directions in the load. It can be noted that the switch S_1 in this case is the only switch that can control the current path. Finally, switch *on* the other two transistors S_5 & S_6 in the three–phase switch that is eventually draining the current as shown in *State* 5, Fig. 2.7(e).

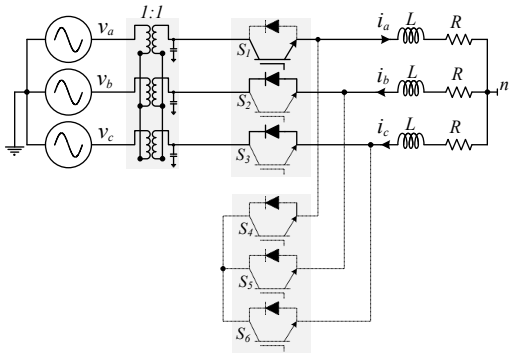
2.3 Second Topology with 12 Switches and 12 Diodes

This topology is shown in Fig. 2.8; each phase in the three–phase voltage source has four switches to perform multiple steps switching technique in a Buck–type AC chopper all the time, while the first topology has only two switches. Therefore, the number of switches has been increased in this topology. Consequently, turning the switches *on* and *off* in this topology requires four control signals only, unlike the previous topology. This topology implements the multiple steps switching technique throughout the entire power period. However, one of the two three–phase switches is *on* for half of the time and is *off* the other half of the time. As mentioned above only one of the twelve transistors drains a current at a particular time in the six cases.

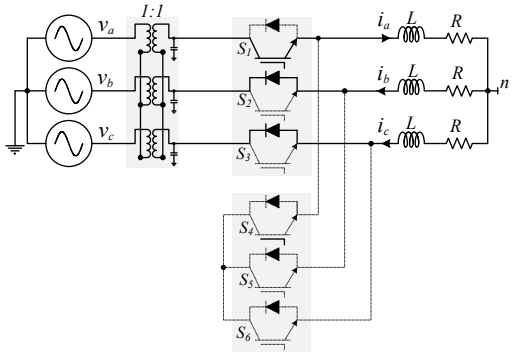
This topology is slightly different from the first topology because the load can be connected to the voltage source by the switches S_1, S_2 & S_3 or by the switches S_7, S_8 & S_9 while the switches S_4 to S_6 & S_{10} to S_{12} are *off*. However, the input voltage source will be disconnected and the load will be shorted by the switches S_4, S_5 & S_6 or the switches S_{10}, S_{11} & S_{12} while the switches S_1 to S_1 & S_7 to S_9 are *off*. On the other hand, when the current is positive in one



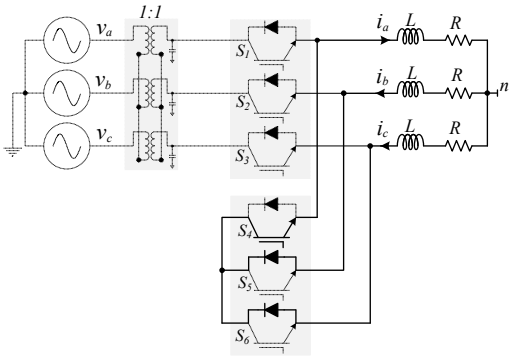
(a) State 1, S_1 is draining a positive current



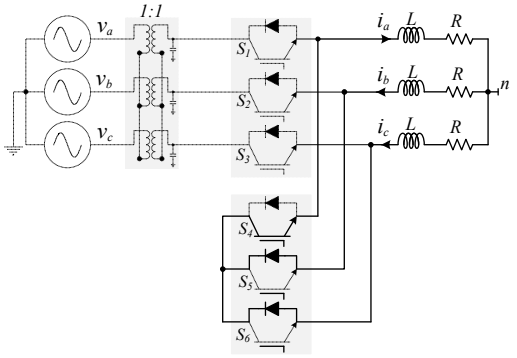
(b) State 2, turn–off S_2 &S_3, the current is flowing through S_1



(c) State 3, turn–on S_4 the transistor S_1 is still draining a positive current



(d) State 4, turn–off S_1, the current path changed and S_4 is draining the current



(e) State 5, turn–on S_5 &S_6, the transistor S_4 is still draining a positive current

Figure 2.7: Switching Process when i_b and i_c are Negative and i_a is Positive

phase and is negative in the other two phases, the switches S_1 to S_6 will conduct the current while the other six switches are *off* during this case. In the other case, when the current is positive in two phases and negative in the other phase, the switches S_7 to S_{12} will conduct the currents while the other six switches are *off* during this case. This pattern guarantees that only one transistor will drain current at a specific time and applies the multiple steps switching technique.

Similar to the previous topology, the switching process depends on the current direction in the load. This topology uses the signals X_1, X_2, X_3 and X_4 that are shown in Fig. 2.2(b) to control the switches and implements the multiple steps switching technique by following the next procedure:

1. Switch *off* the two transistors that are connecting the input voltage source to the load and are not draining any current in the active three–phase

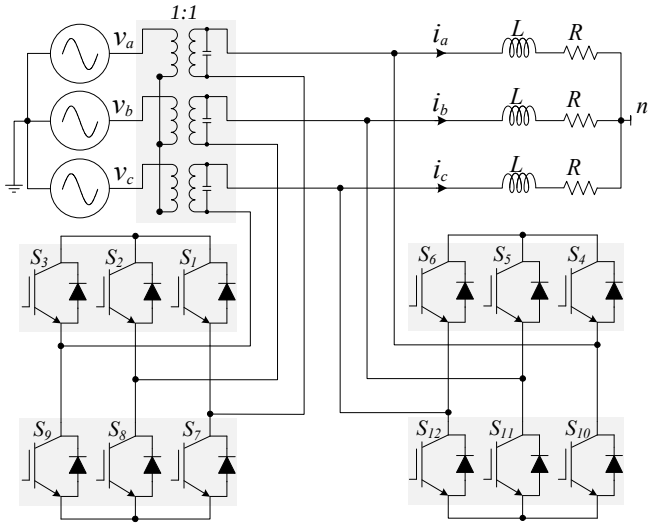


Figure 2.8: Second Topology

switch at present.

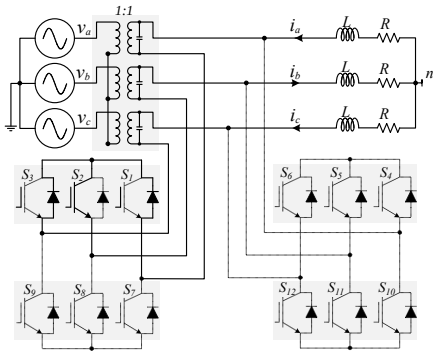
2. Switch *on* the transistor that will disconnect the input voltage source from the load by shorting the load. Also, this switch is in the non–active three–phase switch and it will drain the current in the same direction.

3. Switch *off* the transistor that is currently draining the current in the active three–phase switch. So, the other three–phase switch will be activated as a result and the current will start flowing through the transistor that is already *on* and through the anti–parallel diodes of the other switches.

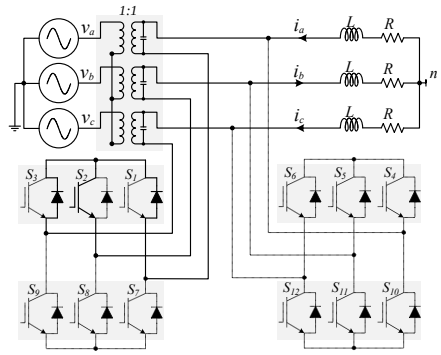
4. Switch *on* the other two transistors in the active three–phase switch.

Taking *case* 4 Fig. 2.1 as an example of this topology, Fig. 2.9 shows the switching process when the current in phases A and C is negative and the current in phase B is positive. In this case, the load is connected to the input voltage source with the switches S_1, S_2 & S_3 while all the other switches are *off*. Following the procedure mentioned above, the two transistors that are not draining any current in this case are S_1 & S_3. Thus, *State* 1 in Fig. 2.9(a) shows the load connected to the input voltage source with the switches S_1, S_2 & S_3 while the other switches are *off*. Although S_1 & S_3 are *on*, the transistors are not draining any current. However, in *State* 2 Fig. 2.9(b) after switching *off* S_1 & S_3, S_2 is the only transistor draining current. To keep the current flowing in the same direction, S_5 should be switched *on* before disconnecting the input voltage source from the load as in *State* 3 Fig. 2.9(c). In *State* 4, Fig. 2.9(d) switching *off* the transistor that is presently draining the current which is S_2, will immediately change the current path by making a short on the load and

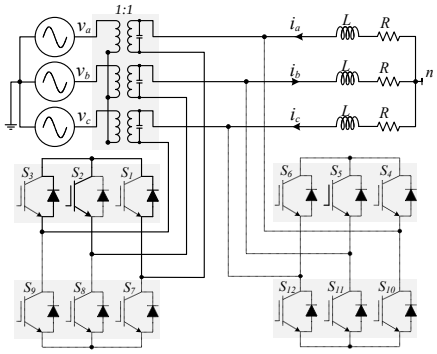
keeping the currents flowing in the same directions in the load. It can be noted that the switch S_2, in this case, is the only switch that can control the current path. Finally, switch *on* the other two transistors S_5 & S_6 in the three–phase switch that is eventually draining the current as shown in *State* 5, Fig. 2.9(e). Significantly, in all the *States* there is only one transistor draining current.



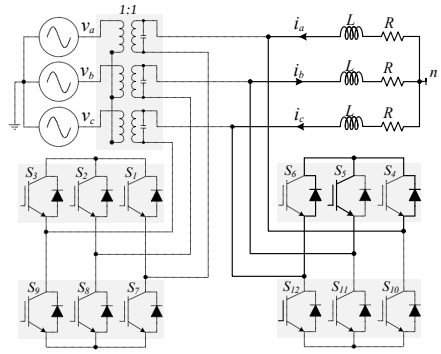
(a) State 1, S_2 is draining a positive current



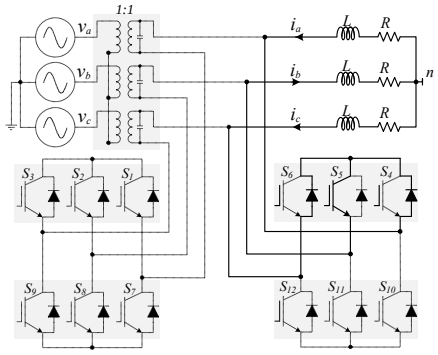
(b) State 2, turn–off S_1 &S_3, the current is flowing through S_2



(c) State 3, turn–on S_5 the transistor S_2 is still draining a positive current



(d) State 4, turn–off S_2, the current path changed and S_5 is draining the current



(e) State 5, turn–on S_4 &S_6, S_5 is still draining a positive current

Figure 2.9: Switching Process when i_{a} and i_{c} are Negative and i_{b} is Positive

2.4 Third Topology with 2 Switches and 14 Diodes

The topology is shown in Fig. 2.10. This topology uses only two driving switches S_1 and S_2 which makes the switching strategy easy. These two switches are used to connect the load to the three–phase source and disconnect it as well. So, when one of the two switches is *on*, the other one should be *off* and vice versa. In addition, both switches can not be closed at the same time, because this will short the input voltage source. Also, they can not be open at the same time, because the inductor's current path should not be open.

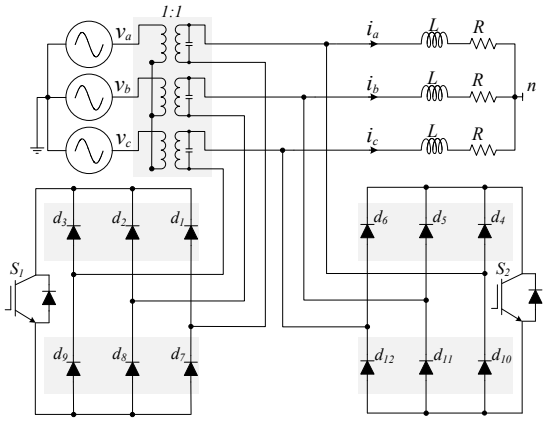


Figure 2.10: Third Topology

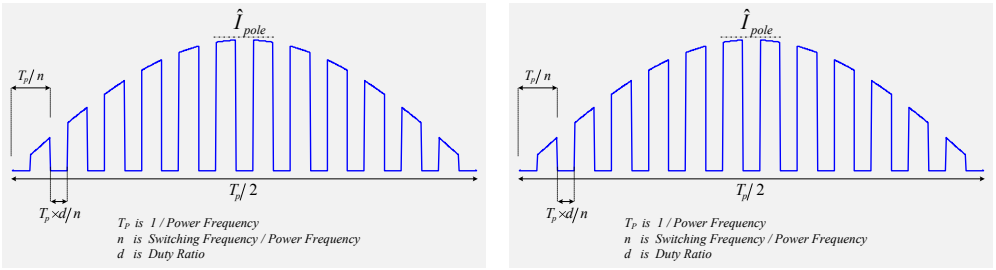
Also, there is no multiple steps switching technique that can be applied in this topology but each of the switches S_1 and S_2 is realized using a Diode–Bridge and only one active switch.

3. Average & RMS Currents

In this chapter the average and RMS currents for the switches beside the AC source will be presented in general formulas for the three topologies as follows:

3.1 First Topology [6 switches and 6 diodes]

The shapes of the waveforms in this topology are shown in Fig. 3.1.



(a) Current through the Diode (b) Current through the Transistor

Figure 3.1: Current Waveforms of the Switches.

3.1.1 Average Diode Current

$$< I_{\mathrm{d}} >= \frac{\hat{I}_{\mathrm{Pole}}}{T_{\mathrm{P}}} \sum_{i=0}^{n/2} \left\{ \int_{i\frac{T_{\mathrm{P}}}{n}}^{(\frac{T_{\mathrm{P}} \times d}{n} + i\frac{T_{\mathrm{P}}}{n})} sin(\frac{2\pi}{T_{\mathrm{P}}} \times t) \cdot dt \right\} \tag{3.1}$$

Where

$$\sum_{i=0}^{n} cos(ai) = \frac{sin(\frac{a}{2}(n+1)) \times cos(\frac{a}{2}n)}{sin(\pi/n)} \tag{3.2}$$

$$\sum_{i=0}^{n} sin(ai) = \frac{sin(\frac{a}{2}(n+1)) \times sin(\frac{a}{2}n)}{sin(\pi/n)} \tag{3.3}$$

$$< I_{\mathrm{d}} >= \frac{\hat{I}_{\mathrm{Pole}}}{2\pi}\left[\frac{sin(\frac{2\pi d}{n}) \times cos(\frac{\pi}{n})}{sin(\frac{\pi}{n})}\right] \tag{3.4}$$

3.1.2 RMS Diode Current

$$I^2_{\mathrm{d_{rms}}} = \frac{\hat{I}^2_{\mathrm{Pole}}}{T_P}\sum_{i=0}^{n/2}\left\{\int_{i\frac{T_{\mathrm{P}}}{n}}^{(\frac{T_{\mathrm{P}}\times d}{n}+i\frac{T_{\mathrm{P}}}{n})} sin^2(\frac{2\pi}{T_{\mathrm{P}}}\times t)\cdot dt\right\} \tag{3.5}$$

$$I_{\mathrm{d_{rms}}} = \hat{I}_{\mathrm{Pole}}\left[\frac{d}{4}+\frac{d}{2n}-\frac{1}{8\pi}sin(\frac{4\pi d}{n})\right]^{1/2} \tag{3.6}$$

Note that the shape of the switch current in this topology is the same as the shape of diode current .

3.1.3 Average Transistor Current

$$< I_m rd >= \frac{\hat{I}_{\mathrm{Pole}}}{T_{\mathrm{P}}}\sum_{i=0}^{n/2}\left\{\int_{i\frac{T_{\mathrm{P}}}{n}}^{(\frac{T_{\mathrm{P}}\times d}{n}+i\frac{T_{\mathrm{P}}}{n})} sin(\frac{2\pi}{T_{\mathrm{P}}}\times t)\cdot dt\right\} \tag{3.7}$$

$$< I_{\mathrm{d}} >= \frac{\hat{I}_{\mathrm{Pole}}}{2\pi}\left[\frac{sin(\frac{2\pi d}{n}) \times cos(\frac{\pi}{n})}{sin(\frac{\pi}{n})}\right] \tag{3.8}$$

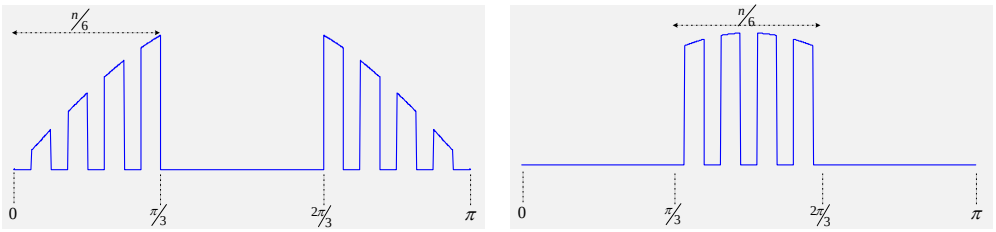
3.1.4 RMS Transistor Current

$$I^2_{\mathrm{d_{rms}}} = \frac{\hat{I}^2_{\mathrm{Pole}}}{T_{\mathrm{P}}}\sum_{i=0}^{n/2}\left\{\int_{i\frac{T_{\mathrm{P}}}{n}}^{(\frac{T_{\mathrm{P}}\times d}{n}+i\frac{T_{\mathrm{P}}}{n})} sin^2(\frac{2\pi}{T_{\mathrm{P}}}\times t)\cdot dt\right\} \tag{3.9}$$

$$I_{\mathrm{t_{rms}}} = \hat{I}_{\mathrm{Pole}}\left[\frac{d}{4}+\frac{d}{2n}-\frac{1}{8\pi}sin(\frac{4\pi d}{n})\right]^{1/2} \tag{3.10}$$

3.2 Second Topology [12 switches and 12 diodes]

The shapes of the waveforms in this topology are shown in Fig. 3.2.



(a) Current through the Diode (b) Current through the Transistor

Figure 3.2: Current Waveforms of the Switches.

3.2.1 Average Diode Current

$$< I_{\mathrm{d}} >= \frac{\hat{I}_{\mathrm{Pole}}}{T_{\mathrm{P}}} \sum_{i=0}^{n/6} \left\{ \int_{i\frac{T_{\mathrm{P}}}{n}}^{(\frac{T_{\mathrm{P}}\times d}{n}+i\frac{T_{\mathrm{P}}}{n})} sin(\frac{2\pi}{T_{\mathrm{P}}} \times t) \cdot dt \right\} \tag{3.11}$$
$$+ \frac{\hat{I}_{\mathrm{Pole}}}{T_{\mathrm{P}}} \sum_{i=0}^{n/6} \left\{ \int_{(\frac{2\pi}{3}+i\frac{T_{\mathrm{P}}}{n})}^{(\frac{2\pi}{3}+\frac{T_{\mathrm{P}}\times d}{n}+i\frac{T_{\mathrm{P}}}{n})} sin(\frac{2\pi}{T_{\mathrm{P}}} \times t) \cdot dt \right\}$$

$$< I_{\mathrm{d}} >= \frac{\hat{I}_{\mathrm{Pole}}}{2\pi} \left[\frac{sin(\frac{\pi}{6}+\frac{\pi}{n}) \times sin(\frac{2\pi d}{n})}{sin(\frac{\pi}{n})} \right] \tag{3.12}$$

3.2.2 RMS Diode Current

$$I\mathrm{d}_{\mathrm{rms}}{}^2 = \frac{\hat{I}^2_{\mathrm{Pole}}}{T_{\mathrm{P}}} \sum_{i=0}^{n/6} \left\{ \int_{i\frac{T_{\mathrm{P}}}{n}}^{(\frac{T_{\mathrm{P}}\times d}{n}+i\frac{T_{\mathrm{P}}}{n})} sin^2(\frac{2\pi}{T_{\mathrm{P}}} \times t) \cdot dt \right\} \tag{3.13}$$
$$+ \frac{\hat{I}^2_{\mathrm{Pole}}}{T_{\mathrm{P}}} \sum_{i=0}^{n/6} \left\{ \int_{(\frac{2\pi}{3}+i\frac{T_{\mathrm{P}}}{n})}^{(\frac{2\pi}{3}+\frac{T_{\mathrm{P}}\times d}{n}+i\frac{T_{\mathrm{P}}}{n})} sin^2(\frac{2\pi}{T_{\mathrm{P}}} \times t) \cdot dt \right\}$$

$$I_{\mathrm{d_{rms}}} = \hat{I}_{\mathrm{Pole}} \left[\frac{d}{6} + \frac{d}{n} - \frac{1}{8\pi} \frac{sin(\frac{\pi}{3} + \frac{2\pi}{n}) \times sin(\frac{4\pi d}{n})}{sin(\frac{2\pi}{n})} \right]^{1/2} \tag{3.14}$$

3.2.3 Average Transistor Current

$$< I_{\mathrm{t}} >= \frac{\hat{I}_{\mathrm{Pole}}}{T_{\mathrm{P}}} \sum_{i=0}^{n/6} \left\{ \int_{(\frac{\pi}{3}+i\frac{T_{\mathrm{P}}}{n})}^{(\frac{\pi}{3}+\frac{T_{\mathrm{P}}\times d}{n}+i\frac{T_{\mathrm{P}}}{n})} sin(\frac{2\pi}{T_{\mathrm{P}}} \times t) \cdot dt \right\} \tag{3.15}$$

$$< I_{\mathrm{t}} >= \frac{\hat{I}_{\mathrm{Pole}}}{2\pi} \left[\frac{sin(\frac{2\pi d}{n}) \times sin(\frac{\pi}{6} + \frac{\pi}{n})}{sin(\frac{\pi}{n})} \right] \tag{3.16}$$

3.2.4 RMS Transistor Current

$$I^2_{\mathrm{t_{rms}}} = \frac{\hat{I}^2_{\mathrm{Pole}}}{T_{\mathrm{P}}} \sum_{i=0}^{n/6} \left\{ \int_{(\frac{\pi}{3}+i\frac{T_{\mathrm{P}}}{n})}^{(\frac{\pi}{3}+\frac{T_{\mathrm{P}}\times d}{n}+i\frac{T_{\mathrm{P}}}{n})} sin^2(\frac{2\pi}{T_{\mathrm{P}}} \times t) \cdot dt \right\} \tag{3.17}$$

$$I_{\mathrm{t_{rms}}} = \hat{I}_{\mathrm{Pole}} \left[\frac{d}{12} + \frac{d}{2n} + \frac{1}{8\pi} \frac{sin(\frac{\pi}{3} + \frac{2\pi}{n}) \times sin(\frac{4\pi d}{n})}{sin(\frac{2\pi}{n})} \right]^{1/2} \tag{3.18}$$

3.3 Third Topology [2 Switches and 14 Diodes]

The shapes of the waveforms in this topology are shown in Fig. 3.3.

3.3.1 Average Diode Current

$$< I_{\mathrm{d}} >= \frac{\hat{I}_{\mathrm{Pole}}}{T_{\mathrm{P}}} \sum_{i=0}^{n/2} \left\{ \int_{i\frac{T_{\mathrm{P}}}{n}}^{(\frac{T_{\mathrm{P}}\times d}{n}+i\frac{T_{\mathrm{P}}}{n})} sin(\frac{2\pi}{T_{\mathrm{P}}} \times t) \cdot dt \right\} \tag{3.19}$$

$$< I_{\mathrm{d}} >= \frac{\hat{I}_{\mathrm{Pole}}}{2\pi} \left[\frac{sin(\frac{2\pi d}{n}) \times cos(\frac{\pi}{n})}{sin(\frac{\pi}{n})} \right] \tag{3.20}$$

3.3.2 RMS Diode Current

$$I_{\mathrm{d_{rms}}}^2 = \frac{\hat{I}_{\mathrm{Pole}}^2}{T_{\mathrm{P}}} \sum_{i=0}^{n/2} \left\{ \int_{i\frac{T_{\mathrm{P}}}{n}}^{(\frac{T_{\mathrm{P}}\times d}{n}+i\frac{T_{\mathrm{P}}}{n})} sin^2(\frac{2\pi}{T_{\mathrm{P}}} \times t) \cdot dt \right\} \tag{3.21}$$

$$I_{\mathrm{d_{rms}}} = \hat{I}_{\mathrm{Pole}} \left[\frac{d}{4} + \frac{d}{2n} - \frac{1}{8\pi} sin(\frac{4\pi d}{n}) \right]^{1/2} \tag{3.22}$$

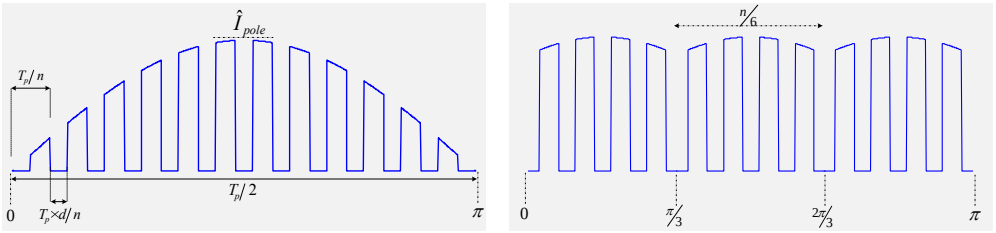
3.3.3 Average Transistor Current

$$< I_{\mathrm{t}} >= \frac{\hat{I}_{\mathrm{Pole}}}{\pi/3} \sum_{i=0}^{n/6} \left\{ \int_{(\frac{\pi}{3}+i\frac{T_{\mathrm{P}}}{n})}^{(\frac{\pi}{3}+\frac{T_{\mathrm{P}}\times d}{n}+i\frac{T_{\mathrm{P}}}{n})} sin(\frac{2\pi}{T_{\mathrm{P}}} \times t) \cdot dt \right\}. \tag{3.23}$$

$$< I_{\mathrm{t}} >= \frac{\hat{I}_{\mathrm{Pole}}}{\pi/3} \left[\frac{sin(\frac{2\pi d}{n}) \times sin(\frac{\pi}{6}+\frac{\pi}{n})}{sin(\frac{\pi}{n})} \right] \tag{3.24}$$

3.3.4 RMS Transistor Current

$$I_{\mathrm{t_{rms}}}^2 = \frac{\hat{I}_{\mathrm{Pole}}^2}{\pi/3} \sum_{i=0}^{n/6} \left\{ \int_{(\frac{\pi}{3}+i\frac{T_{\mathrm{P}}}{n})}^{(\frac{\pi}{3}+\frac{T_{\mathrm{P}}\times d}{n}+i\frac{T_{\mathrm{P}}}{n})} sin^2(\frac{2\pi}{T_{\mathrm{P}}} \times t) \cdot dt \right\} \tag{3.25}$$



(a) Current through the Diode (b) Current through the Transistor

Figure 3.3: Current Waveforms of the Switches

$$I_{t_{\text{rms}}} = \sqrt{6}\hat{I}_{\text{Pole}}\left[\frac{d}{12} + \frac{d}{2n} + \frac{1}{8\pi}\frac{sin(\frac{\pi}{3}+\frac{2\pi}{n}) \times sin(\frac{4\pi d}{n})}{sin(\frac{2\pi}{n})}\right]^{1/2} \tag{3.26}$$

Table 3.1: Average and RMS currents for the three topologies

Topology	**Device**	**Current**	**Formula**
1	Diode	I_{ave}	$\frac{\hat{I}_{\text{Pole}}}{2\pi}\left[\frac{sin(\frac{2\pi d}{n}).cos(\frac{\pi}{n})}{sin(\frac{\pi}{n})}\right]$
	Diode	I_{rms}	$\hat{I}_{\text{Pole}}\left[\frac{d}{4} + \frac{d}{2n} - \frac{1}{8\pi}sin(\frac{4\pi d}{n})\right]^{1/2}$
	Transistor	I_{ave}	$\frac{\hat{I}_{\text{Pole}}}{2\pi}\left[\frac{sin(\frac{2\pi d}{n}).cos(\frac{\pi}{n})}{sin(\frac{\pi}{n})}\right]$
	Transistor	I_{rms}	$\hat{I}_{\text{Pole}}\left[\frac{d}{4} + \frac{d}{2n} - \frac{1}{8\pi}sin(\frac{4\pi d}{n})\right]^{1/2}$
2	Diode	I_{ave}	$\frac{\hat{I}_{\text{Pole}}}{2\pi}\left[\frac{sin(\frac{\pi}{6}-\frac{\pi}{n})\times sin(\frac{2\pi d}{n})}{sin(\frac{\pi}{n})}\right]$
	Diode	I_{rms}	$\hat{I}_{\text{Pole}}\left[\frac{d}{6} + \frac{d}{n} - \frac{1}{8\pi}\frac{sin(\frac{\pi}{3}+\frac{2\pi}{n})\times sin(\frac{4\pi d}{n})}{sin(\frac{2\pi}{n})}\right]^{1/2}$
	Transistor	I_{ave}	$\frac{\hat{I}_{\text{Pole}}}{2\pi}\left[\frac{sin(\frac{2\pi d}{n})\times sin(\frac{\pi}{6}+\frac{\pi}{n})}{sin(\frac{\pi}{n})}\right]$
	Transistor	I_{rms}	$\hat{I}_{\text{Pole}}\left[\frac{d}{12} + \frac{d}{2n} + \frac{1}{8\pi}\frac{sin(\frac{\pi}{3}+\frac{2\pi}{n})\times sin(\frac{4\pi d}{n})}{sin(\frac{2\pi}{n})}\right]^{1/2}$
3	Diode	I_{ave}	$\frac{\hat{I}_{\text{Pole}}}{2\pi}\left[\frac{sin(\frac{2\pi d}{n})\times cos(\frac{\pi}{n})}{sin(\frac{\pi}{n})}\right]$
	Diode	I_{rms}	$\hat{I}_{\text{Pole}}\left[\frac{d}{4} + \frac{d}{2n} - \frac{1}{8\pi}sin(\frac{4\pi d}{n})\right]^{1/2}$
	Transistor	I_{ave}	$\frac{\hat{I}_{\text{Pole}}}{\pi/3}\left[\frac{sin(\frac{2\pi d}{n})\times sin(\frac{\pi}{6}+\frac{\pi}{n})}{sin(\frac{\pi}{n})}\right]$
	Transistor	I_{rms}	$\sqrt{6}\hat{I}_{\text{Pole}}\left[\frac{d}{12} + \frac{d}{2n} + \frac{1}{8\pi}\frac{sin(\frac{\pi}{3}+\frac{2\pi}{n})\times sin(\frac{4\pi d}{n})}{sin(\frac{2\pi}{n})}\right]^{1/2}$

The formulas in the Table 3.1 present the average and RMS currents for the devices that connect the load to the source. However, the other devices use the same formulas after changing (d) to (1-d).

4. Switching Losses Calculations

The switching loss depends on the energy dissipated at every switching event for both transistor and diode semiconductors, so the switching energy in semiconductors is usually assumed to be proportional to the conducting current and the blocking voltage at each switching event as follows [12],

$$E_{\mathrm{i}} = \frac{E^{\mathrm{R}}}{V^{\mathrm{R}} I^{\mathrm{R}}} v_{\mathrm{i}} i_{\mathrm{i}} \tag{4.1}$$

where $\mathrm{E^R}$, $\mathrm{V^R}$ and $\mathrm{I^R}$ represent the reference values of the energy loss, the blocking voltage, and the conducting current respectively. These values are usually on the manufacturer's datasheets. Therefore, the total power loss over one power period is as follows:

$$P_{\mathrm{S}} = F_{\mathrm{p}} \sum_{\mathrm{i}} E_{\mathrm{i}} \tag{4.2}$$

In both topologies that are shown in Fig. 4.1 and Fig. 4.3, the blocking voltage is line–line voltage and the conducting current is the pole current multiplied by the duty ratio.

Before calculating the losses there are some considerations which have to be taken into account. These considerations concern the switching losses for the diodes at turn–on and turn–off events. First of all, the diodes have no turn–on switching losses, because when the transistor is on (carrying the current), the current through the diode is zero. Therefore, at turn–on there is no switching loss. More accurately, the diode blocks the current when it is reverse biased. In

the case of a silicon diode, for example, when it is forward biased, it does not drain any current until 0.7V is applied across it, so when the diode is turned on it will drain a current; however, the voltage across the diode will not drop more than 0.7V, even though the input voltage of the converter is greater. Consequently, the switching losses for the diodes are negligible.

Secondly, the diodes have switching losses at the turn–off event, but this is a function of the voltage they are blocking and the reverse recovery current (not the load current). Precisely, the reverse recovery in the diode occurs when a negative voltage is applied across the diode. In other words, when the diode is in a forward conduction (load current), it will stop conducting at the moment when a negative voltage is applied across the terminals of the diode forcing the diode to turn off. Hence, in comparison with the transistor switching losses which are a function of the line–line voltage and the load current, turn–off losses in the diodes represent a small amount of power. Finally, in this chapter, the dead time is not considered for the switch that has hard switching and there are no switching losses for the diodes in the three examined topologies.

In the topology shown in Fig. 4.1, the transistors t_1, t_2 and t_3 have a hard switching for half of the power period ($\frac{T_\mathrm{p}}{2} = \pi$), whenever the current is positive as shown in Fig. 4.2. On the other hand, the transistors t_4, t_5 and t_6 have hard switching only for a sixth of the power period ($\frac{T_\mathrm{p}}{6} = \frac{\pi}{3}$).

In the topology shown in Fig. 4.3, the transistors t_1, t_2, t_3, t_7, t_8, and t_9, by the voltage source, have hard switching for a sixth of the power period ($\frac{T_\mathrm{p}}{6} = \frac{\pi}{3}$), as shown in Fig. 4.4 and Fig. 4.5. However, the other transistors have

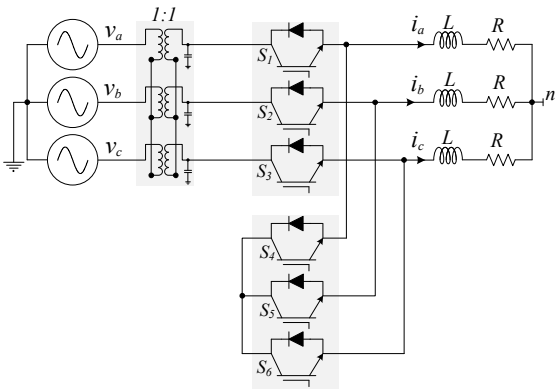


Figure 4.1: First Topology

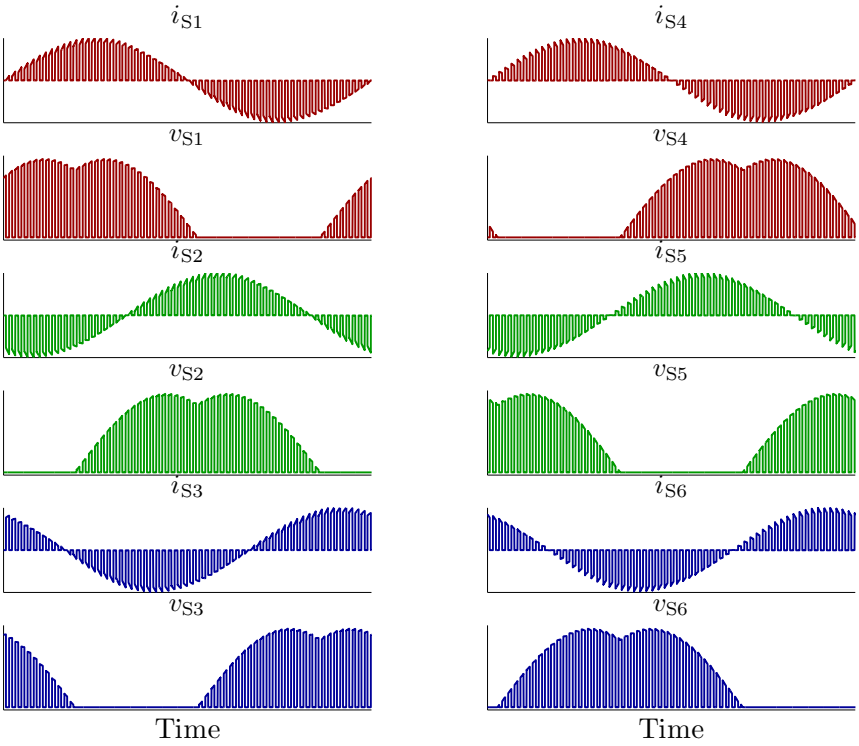


Figure 4.2: Switching Currents and Blocking Voltage

soft switching as shown in Fig. 4.4 and Fig. 4.5.

In the topology shown in Fig. 4.6, the transistors t_1, and t_2 have hard switching during the entire power period.

The devices connected to phase A in the topology shown in Fig. 4.1 are t_1 and t_4. The stem plot for the product of the current and the voltage for the transistors t_1 and t_4 at the turn–on and turn–off events is shown in Fig. 4.8. Also, the product of the current and the voltage in the other phases B and C will be the same.

The topology shown in Fig. 4.3 has four transistors which are connected to phase A. Fig. 4.9 shows the stem plot for the product of the current and the voltage for the transistors t_1, t_4, t_7 and t_{10} at the turn–on and turn–off events. Also, the product of the current and the voltage in the other phases B and C

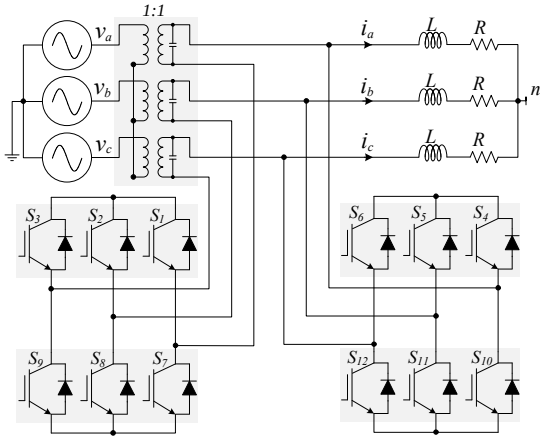


Figure 4.3: Second Topology

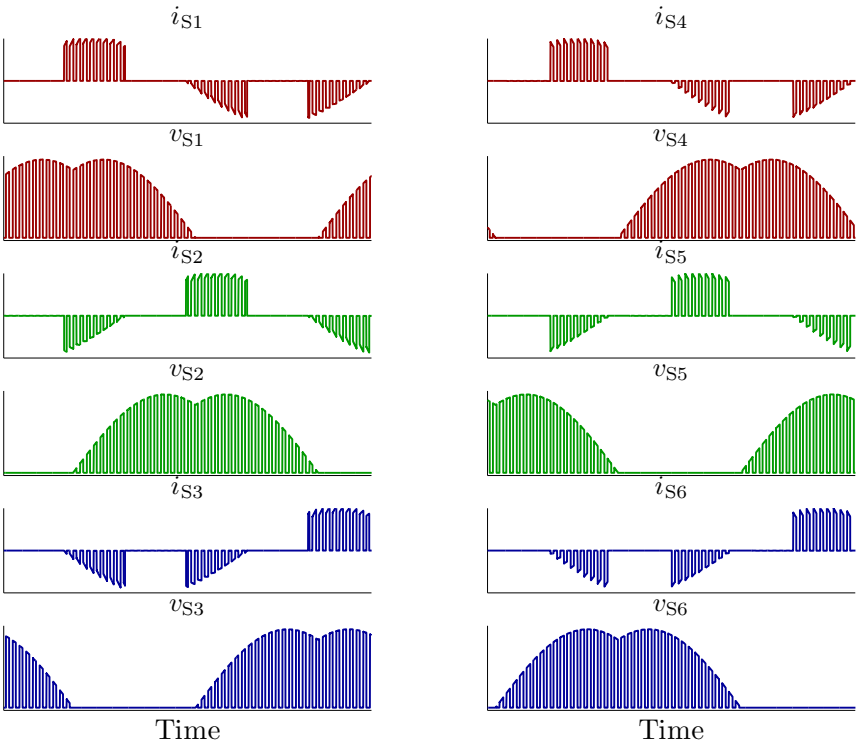


Figure 4.4: Switching Currents and Blocking Voltage

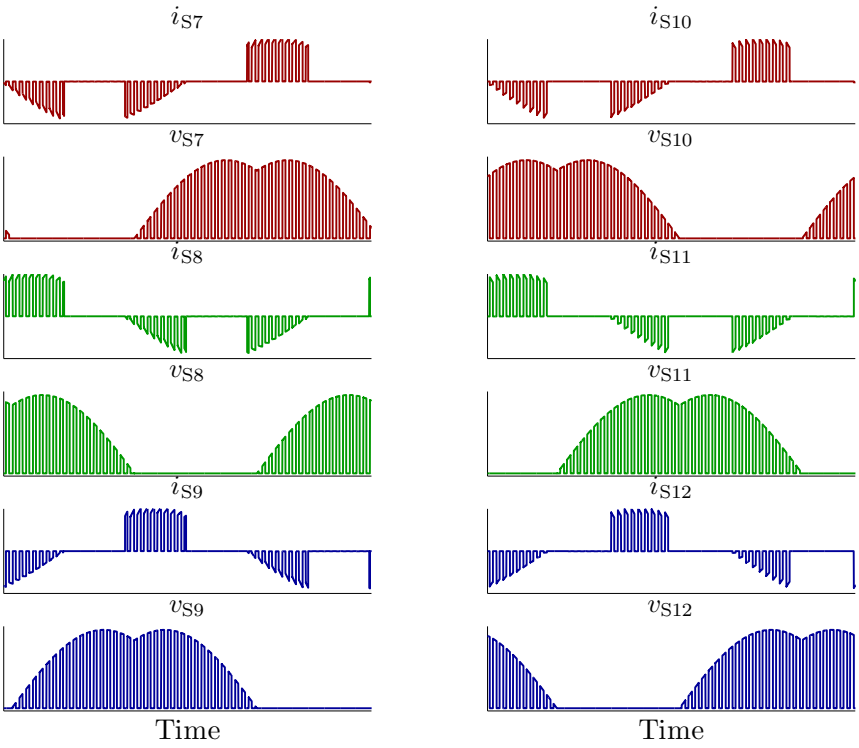


Figure 4.5: Switching Currents and Blocking Voltage

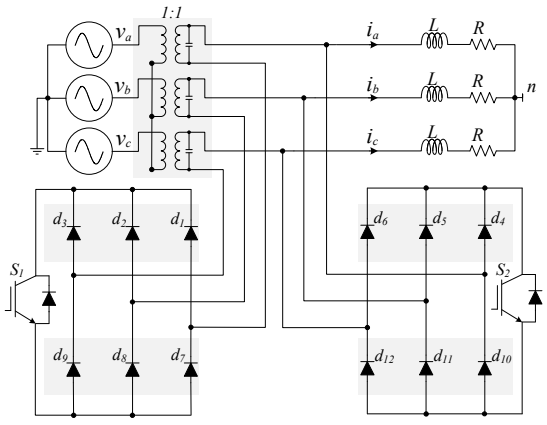


Figure 4.6: Third Proposed Topology

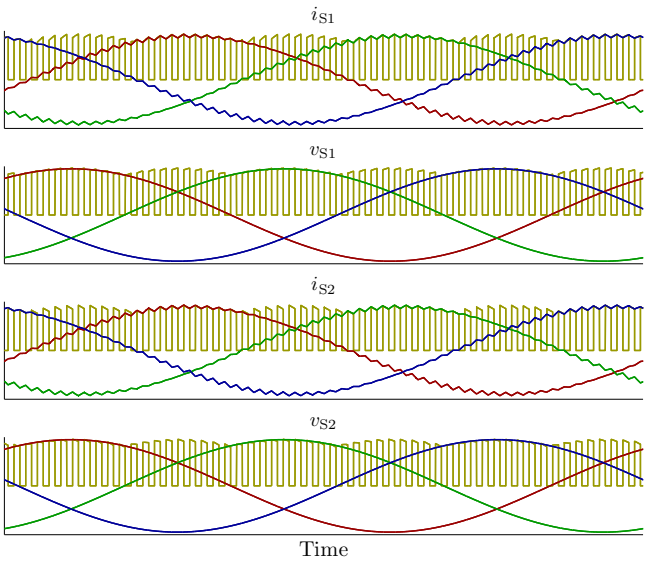


Figure 4.7: Switching Currents and Blocking Voltage

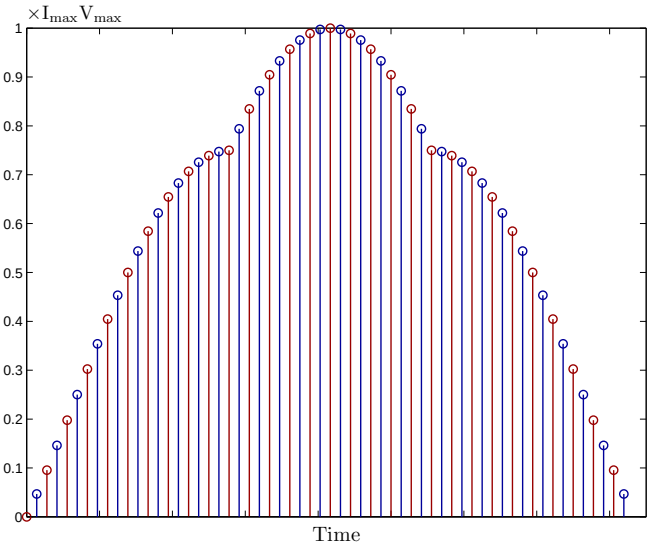


Figure 4.8: Stem Plot for $V_{\mathrm{i}}I_{\mathrm{i}}$ of t_1 and t_4 in the Topology Fig. 4.1

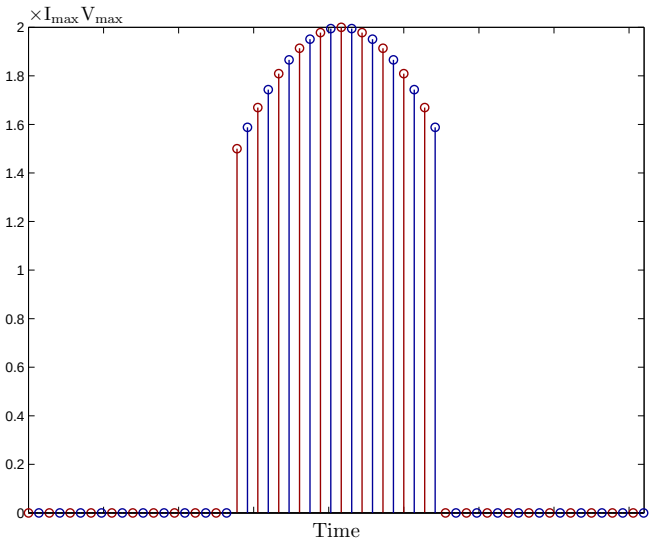


Figure 4.9: Stem Plot for $V_{\mathrm{i}}I_{\mathrm{i}}$ of t_1, t_7, t_4 and t_{10} in the Topology Fig. 2.8

will be the same.

In the topology shown in Fig. 4.6 there are two transistors in the converter. Fig. 4.10 shows the stem plot for the product of the current and the voltage for only one transistor t_1 at the turn–on and turn–off events. Also, the product of the current and the voltage for the other transistor t_2 will be the same.

Finally, it can be seen from the stem plots in Fig. 4.8 and Fig. 4.9 of the topologies in Fig. 4.1 and Fig. 4.3, respectively, that the shapes are not similar. However, the sum of the product at turn–on and turn–off of the transistors in both topologies is equal. Significantly, the total switching losses in both topologies in Fig. 4.1 and Fig. 4.3 are three times the sum of the stem plot in Fig. 4.8 and Fig. 4.9, respectively, which are equal. For the third topology Fig. 4.6, the total switching losses are twice the sum of the stem plot in Fig. 4.10

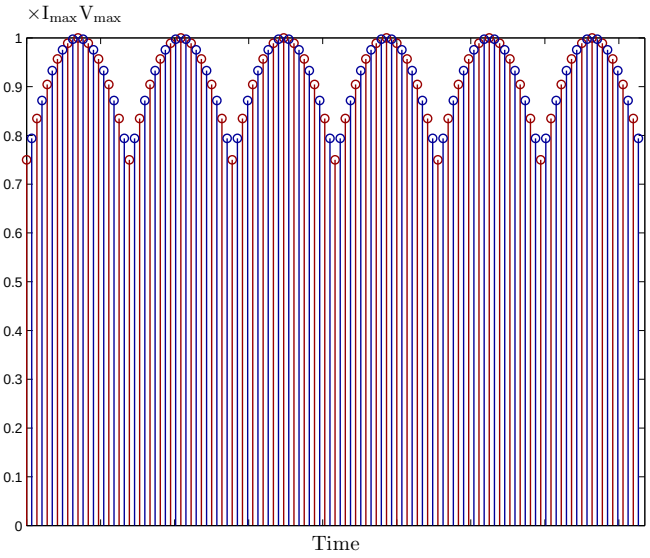


Figure 4.10: Stem Plot for $V_i I_i$ of t_1 in the Topology Fig. 4.6.

because it has only two transistors. Therefore, the total switching losses in the third topology are doubled compared to the total switching losses in the other two topologies.

As mentioned above, it can be seen from (4.1) that the topologies will have the same switching losses only if they are built by similar devices. Actually, the devices are not conducting the same amount of current in the topologies, but they are blocking line–line voltage, so the size of the device will be different in the two topologies which makes the reference values for the energy loss and the conducting current in (4.1) have different values.

Therefore, taking into account the switching losses for each device in the first and second topologies at the turn–on and turn–off events, the analytical formula that expresses the losses has been developed as follows:

$$P_{\mathrm{S}} = 3\frac{F_{\mathrm{p}}\sqrt{1}2V_{\mathrm{in}}V_{\mathrm{out}}}{|Z_{\mathrm{Load}}|}\left[\frac{\mathrm{n}}{3} + \frac{\sqrt{3}}{2sin(\frac{2\pi}{n})}\left[cos(\frac{2\pi}{n}(2d-1)) + cos(\frac{2\pi}{n})\right]\right]\left[\frac{E^{\mathrm{R}}}{V^{\mathrm{R}}I^{\mathrm{R}}}\right] \tag{4.3}$$

However, the analytical formula that expresses the losses for the third topology is as follows:

$$P_{\mathrm{S}} = 6\frac{F_{\mathrm{p}}\sqrt{1}2V_{\mathrm{in}}V_{\mathrm{out}}}{|Z_{\mathrm{Load}}|}\left[\frac{n}{3} + \frac{\sqrt{3}}{2sin(\frac{2\pi}{n})}\left[cos(\frac{2\pi}{n}(2d-1)) + cos(\frac{2\pi}{n})\right]\right]\left[\frac{E^{\mathrm{R}}}{V^{\mathrm{R}}I^{\mathrm{R}}}\right] \tag{4.4}$$

where,

d : duty ratio ($0 \leq d \leq 1$)

V_{in} : rms voltage source

F_{p} : power frequency

Z_{Load} : $R + jX_{\mathrm{L}}$

F_{sw} : switching frequency

n : $\frac{F_{\mathrm{sw}}}{F_{\mathrm{p}}}$

V_{out} : output voltage of the converter which is:

$$V_{\mathrm{out}} = V_{\mathrm{in}}\sqrt{d} \tag{4.5}$$

In comparison, the devices in the topology shown in Fig 4.3 with 12 switches and 12 diodes are conducting less amount of current than the devices in the topology shown in Fig 4.1.

5. Hard Switching versus Semi–Soft Switching

This chapter compares the first two topologies after taking into account the dead–time for the switches that have hard switching and the fact that there are no switching losses for the diodes in both topologies.

In both topologies shown in Fig. 5.1 and Fig. 2.8, the blocking voltage is line–line voltage and the conducting current is the pole current multiplied by the duty ratio.

The conduction loss for the diodes as well as for the transistors is usually modeled by the product of the current through the device and the voltage drop across this device [12]. When the voltage drop across the device is approximated by a linear function depends on the current as in (5.1),

$$v_{\mathrm{on}}(i) = V_{\mathrm{on}} + r_{\mathrm{on}} i \tag{5.1}$$

therefore, the average power loss can be determined in (5.2) as follows:

$$\mathrm{P_C} = V_{\mathrm{on}} \mathrm{I}_{\mathrm{on}}^{\mathrm{avr}} + r_{\mathrm{on}} \left(\mathrm{I}_{\mathrm{on}}^{\mathrm{rms}}\right)^2 \tag{5.2}$$

where V_{on} and r_{on} are usually available on the manufacturer's datasheets.

5.1 Evaluation of Hard Switching Converter

The topology with hard switching is shown in Fig. 5.1. This topology has six switches that are divided into two driving three–phase switches S_α and S_β. These two switches S_α and S_β are used to connect the load to the three–phase source and disconnect it as well. Note that the two three–phase switches can not

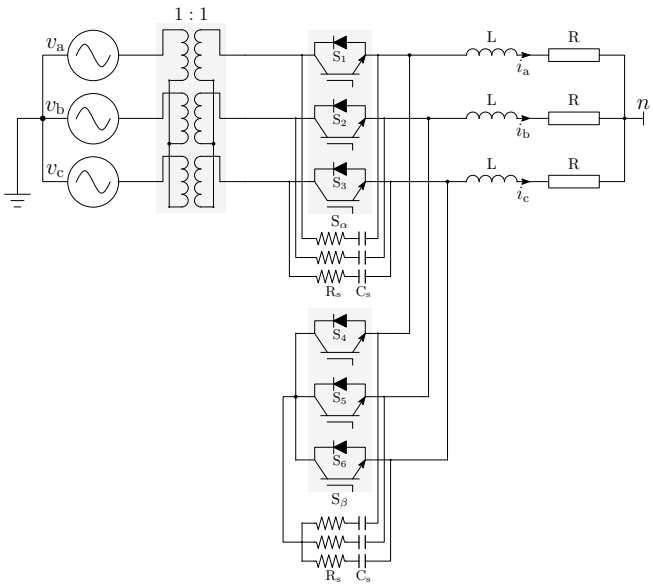


Figure 5.1: Buck–type AC Chopper.

be closed at the same time in this topology because this causes a short circuit on the three phase voltage source. Also, both three–phase switches can not be open at the same time because the load will be disconnected and remains in an open circuit, which may generate voltage spikes [4]. Therefore, in the case of doing hard switching, one of the three–phase switches should be closed while the other switch is open and vice versa. In other words, S_α and S_β switch complementarily as in the DC–DC converters. Consequently, this topology has to have a dead–time and during this time the load current will flow through the snubber circuits and increase the losses especially for the high power converters. In addition, each device needs its own snubber to avoid the voltage spikes during the switching process. This snubber circuit is used to carry the load current during turning off the switch. Therefore, when the switch is turned off the conduction current

will start charging the capacitor in the snubber circuit and the voltage will raise as a result. However, the AC input voltage is chopped by the converter and then filtered to give the output voltage waveform that has the same shape and frequency but a different amplitude which depends on the duty ratio.

Indeed, during the dead–time, which is essential to ensure that there is no short circuit on the source, the load current has no path to go; meanwhile, the load current can not be interrupted. On the other hand, the dead–time must be as narrow as possible to minimize the losses due to voltage spikes at turn–on and turn–off events [18]. Nevertheless, the load current will drain across the snubber circuits increasing the power losses as a result and the snubber circuit will be bulky for such topology.

5.1.1 Switching Losses Calculation

The energy stored in the snubber capacitor C_{s} transfers to the snubber resistor R_{s} and the switch every time it turns on. Also, the inductive load current cannot be changed instantly during turn–off. However, this current diverts through the snubber resistor R_{s} causing voltage spikes as shown in the Fig. 5.3. In general, the loss of the converter mainly includes the power devices conduction loss and switching loss. Since the device data sheet from the manufacturer provides the reference values of the energy loss in (4.1), the power devices switching loss of the converter can be calculated by the following expression:

$$P_{\mathrm{s}} = 3\frac{F_{\mathrm{p}}V_{\mathrm{out}}}{|Z_{\mathrm{Load}}|}\Big\{\sqrt{1}2V_{\mathrm{in}}\left[\frac{n}{3}+\frac{\sqrt{3}}{2sin(\frac{2\pi}{n})}\left[cos(\frac{2\pi}{n}(2d-1))+cos(\frac{2\pi}{n})\right]\right] + \frac{2(Dt/C_{\mathrm{s}}+R_{\mathrm{s}})V_{\mathrm{out}}}{|Z_{\mathrm{Load}}|}\left[\frac{n}{3}-\frac{\sqrt{3}}{2sin(\frac{2\pi}{n})}\left[cos(\frac{2\pi}{n}(2d-1))+\frac{\pi}{3}\right]\right]\Big\}\left[\frac{E^{\mathrm{R}}}{V^{\mathrm{R}}I^{\mathrm{R}}}\right] \tag{5.3}$$

where,

d :	duty ratio ($0 \leq d \leq 1$)	V_{in} :	rms voltage source
F_{p} :	power frequency	C_{s} :	snubber capacitor
F_{sw} :	switching frequency	R_{s} :	snubber resistor
n :	$\frac{F_{\mathrm{sw}}}{F_{\mathrm{p}}}$	Z_{Load} :	$R + jX_{\mathrm{L}}$
Dt :	dead–time	V_{out} :	output voltage

$$V_{\mathrm{out}} = V_{\mathrm{in}}\sqrt{d} \tag{5.4}$$

5.1.2 Conduction Losses Calculation

Depending on the Equation(5.2), the power devices conduction losses of the converter can be calculated as follows:

1- Conduction loss for the diodes that are connected to phase A is:

$$\begin{aligned}\mathrm{CondLoss_{D_1}(d)} &= \mathrm{V_{on_d}} < \mathrm{I} >_{\mathrm{D_1(d)}} + \mathrm{R_{on_d}}\left(\mathrm{I}^{\mathrm{RMS}}_{\mathrm{D_1(d)}}\right)^2 \\ \mathrm{CondLoss_{D_4}(\bar{d})} &= \mathrm{V_{on_d}} < \mathrm{I} >_{\mathrm{D_4(\bar{d})}} + \mathrm{R_{on_d}}\left(\mathrm{I}^{\mathrm{RMS}}_{\mathrm{D_4(\bar{d})}}\right)^2\end{aligned}$$

2- Conduction losses for the transistors that are connected to phase A is:

$$\begin{aligned}\mathrm{CondLoss_{T_1}(d)} &= \mathrm{V_{on_t}} < \mathrm{I} >_{\mathrm{T_1(d)}} + \mathrm{R_{on_t}}\left(\mathrm{I}^{\mathrm{RMS}}_{\mathrm{T_1(d)}}\right)^2 \\ \mathrm{CondLoss_{T_4}(\bar{d})} &= \mathrm{V_{on_t}} < \mathrm{I} >_{\mathrm{T_4(\bar{d})}} + \mathrm{R_{on_t}}\left(\mathrm{I}^{\mathrm{RMS}}_{\mathrm{T_4(\bar{d})}}\right)^2\end{aligned}$$

Therefore, the total conduction losses for the hard switching topology is:

$$\text{Total}_{\text{HS}} = 3 \times \{\text{CondLoss}_{\text{D}_1}(\text{d}) + \text{CondLoss}_{\text{T}_1}(\text{d}) \\ \text{CondLoss}_{\text{D}_4}(\bar{\text{d}}) + \text{CondLoss}_{\text{T}_4}(\bar{\text{d}})\}$$

where,

- $\text{V}_{\text{on}_\text{d}}, \text{R}_{\text{on}_\text{d}}, \text{V}_{\text{on}_\text{t}}$ and $\text{R}_{\text{on}_\text{t}}$ are available on the manufacturer's datasheets.
- d is the duty cycle.
- $\bar{\text{d}} = 1 - \text{d}$.

Table 5.1: Average and RMS currents for the hard switching topology

Topology	**Device**	**Current**	**Formula**
Hard Switching	Diode	I_{ave}	$\frac{\hat{V_{\text{out}}}}{2\pi\lvert Z_{\text{Load}}\rvert}\left[\frac{sin(\frac{2\pi d}{n}).cos(\frac{\pi}{n})}{sin(\frac{\pi}{n})}\right]$
	Diode	I_{rms}	$\frac{\hat{V_{\text{out}}}}{\lvert Z_{\text{Load}}\rvert}\left[\frac{d}{4}+\frac{d}{2n}-\frac{1}{8\pi}sin(\frac{4\pi d}{n})\right]^{1/2}$
	Transistor	I_{ave}	$\frac{\hat{V_{\text{out}}}}{2\pi\lvert Z_{\text{Load}}\rvert}\left[\frac{sin(\frac{2\pi d}{n}).cos(\frac{\pi}{n})}{sin(\frac{\pi}{n})}\right]$
	Transistor	I_{rms}	$\frac{\hat{V_{\text{out}}}}{\lvert Z_{\text{Load}}\rvert}\left[\frac{d}{4}+\frac{d}{2n}-\frac{1}{8\pi}sin(\frac{4\pi d}{n})\right]^{1/2}$

Therefore,

$$\text{P}_\text{C} = 3 \times (\text{V}_{\text{on}_\text{d}} + \text{V}_{\text{on}_\text{t}})\frac{\hat{V_{\text{out}}}}{\pi\lvert Z_{\text{Load}}\rvert}cos(\frac{\pi}{n})cos(\frac{\pi}{n}(2d-1)) + \\ 3 \times (\text{R}_{\text{on}_\text{d}} + \text{R}_{\text{on}_\text{t}})\left(\frac{\hat{V_{\text{out}}}}{\lvert Z_{\text{Load}}\rvert}\right)^2\left[\frac{1}{4}+\frac{1}{2n}-\frac{1}{4\pi}sin(\frac{2\pi}{n})cos(\frac{2\pi}{2}(2d-1))\right] \quad (5.5)$$

5.2 Evaluation of Semi–Soft Switching Converter

The converter shown in Fig. 2.8 presents a new topology of AC chopper with a capability to perform semi–soft switching in multiple steps. Also, the switching technique in this topology is very similar to the four–step semi–soft commutation that has been used in the Matrix Converter (MC) [20]. The advantage of using this technique in the MC is that the switching losses are reduced by 50% compared to the hard switching [20]. On the other hand, the four–step semi–soft commutation in the MC significantly increases the conduction losses. However, the semi–soft topology overcomes the switching problems in the AC chopper converters without increasing the conduction losses of the devices. The switching process in the topology depends on the current direction in the load. Therefore, according to the current direction, there are six different cases or operation modes; each case is 60° as shown in Fig. 2.1.

This topology has four switches in each phase to do a multiple steps switching technique in a Buck–type AC chopper all the time, while the first topology has only two switches in each phase. Therefore, the number of the switches has been increased in this topology. Consequently, turning the switches on and off in this topology needs four control signals. This topology implements the multiple steps switching technique throughout the entire power period. However, one of the two three–phase switches is on for half of the time and is off the other half of the time. Accordingly, only one of the twelve transistors drains current at a particular time in the six cases.

This topology is slightly different from the first topology because the load can be connected to the voltage source by the switches S_1, S_2 & S_3 or the switches S_7, S_8 & S_9 while the switches S_4 to S_6 & S_{10} to S_{12} are off. However, the input voltage source will be disconnected and the load will be shorted by the switches S_4, S_5 & S_6 or the switches S_{10}, S_{11} & S_{12} while the switches S_1 to S_1 & S_7 to S_9 are off. On the other hand, when the current is positive in one phase and negative in the other two phases, the switches S_1 to S_6 will conduct the currents while the other six switches are off during this case. In the other case, when the current is positive in two phases and is negative in the other phase, the switches S_7 to S_{12} will conduct the currents while the other six switches are off during this case. This pattern guarantees that only one transistor will drain current at a specific time and applies the multiple steps switching technique.

The switching process that depends on the current direction in this converter has been explained in Chapter 2

5.2.1 Switching Losses Calculation

There is no snubber circuit in the semi–soft topology that is shown in Fig 2.8. Following the multiple steps switching technique, creates a path for the current. This current flows during the switching events as it shown in Fig 2.9 Chapter 2. Then, taking into account the same considerations that applied in the hard switching topology, the analytical formula that expresses the switching losses in the semi–soft topology can be developed as follows:

$$P_{\mathrm{S}} = 3\frac{F_{\mathrm{p}}\sqrt{1}2V_{\mathrm{in}}V_{\mathrm{out}}}{|Z_{\mathrm{Load}}|}\left[\frac{\mathrm{n}}{3} + \frac{\sqrt{3}}{2sin(\frac{2\pi}{n})}\left[cos(\frac{2\pi}{n}(2d-1)) + cos(\frac{2\pi}{n})\right]\right]\left[\frac{E^{\mathrm{R}}}{V^{\mathrm{R}}I^{\mathrm{R}}}\right] \tag{5.6}$$

where,

d : duty ratio ($0 \leq d \leq 1$) $\quad$ V_{in} : rms voltage source

F_{p} : power frequency $\quad$ Z_{Load} : $R + jX_{\text{L}}$

F_{sw} : switching frequency $\quad$ n : $\frac{F_{\text{sw}}}{F_{\text{p}}}$

V_{out} : output voltage of the converter which is:

$$V_{\text{out}} = V_{\text{in}}\sqrt{d} \tag{5.7}$$

5.2.2 Conduction Losses Calculation

Depending on the Equation(5.2), the power devices conduction losses of the converter can be calculated as follows:

1- Conduction loss for the diodes that are connected to phase A is:

$$\begin{aligned}
\text{CondLoss}_{\text{D}_1+\text{D}_7}(\text{d}) &= \text{V}_{\text{on}_\text{d}} < \text{I} >_{\text{D}_1(\text{d})} + \text{R}_{\text{on}_\text{d}} \left(\text{I}^{\text{RMS}}_{\text{D}_1(\text{d})}\right)^2 \\
&+ \text{V}_{\text{on}_\text{d}} < \text{I} >_{\text{D}_7(\text{d})} + \text{R}_{\text{on}_\text{d}} \left(\text{I}^{\text{RMS}}_{\text{D}_7(\text{d})}\right)^2 \\
&= 2 \times \left[\text{V}_{\text{on}_\text{d}} < \text{I} >_{\text{D(d)}} + \text{R}_{\text{on}_\text{d}} \left(\text{I}^{\text{RMS}}_{\text{D(d)}}\right)^2\right] \\
\text{CondLoss}_{\text{D}_4+\text{D}_{10}}(\bar{\text{d}}) &= \text{V}_{\text{on}_\text{d}} < \text{I} >_{\text{D}_4(\bar{\text{d}})} + \text{R}_{\text{on}_\text{d}} \left(\text{I}^{\text{RMS}}_{\text{D}_4(\bar{\text{d}})}\right)^2 \\
&+ \text{V}_{\text{on}_\text{d}} < \text{I} >_{\text{D}_{10}(\bar{\text{d}})} + \text{R}_{\text{on}_\text{d}} \left(\text{I}^{\text{RMS}}_{\text{D}_{10}(\bar{\text{d}})}\right)^2 \\
&= 2 \times \left[\text{V}_{\text{on}_\text{d}} < \text{I} >_{\text{D}(\bar{\text{d}})} + \text{R}_{\text{on}_\text{d}} \left(\text{I}^{\text{RMS}}_{\text{D}(\bar{\text{d}})}\right)^2\right]
\end{aligned}$$

2- Conduction losses for the transistors that are connected to phase A is:

$$\begin{aligned}
\text{CondLoss}_{\text{T}_1+\text{T}_7}(\text{d}) &= \text{V}_{\text{on}_\text{t}} < \text{I} >_{\text{T}_1(\text{d})} + \text{R}_{\text{on}_\text{t}} \left(\text{I}^{\text{RMS}}_{\text{T}_1(\text{d})}\right)^2 \\
&+ \text{V}_{\text{on}_\text{t}} < \text{I} >_{\text{T}_7(\text{d})} + \text{R}_{\text{on}_\text{t}} \left(\text{I}^{\text{RMS}}_{\text{T}_7(\text{d})}\right)^2 \\
&= 2 \times \left[\text{V}_{\text{on}_\text{t}} < \text{I} >_{\text{T(d)}} + \text{R}_{\text{on}_\text{t}} \left(\text{I}^{\text{RMS}}_{\text{T(d)}}\right)^2\right] \\
\text{CondLoss}_{\text{T}_4+\text{T}_{10}}(\bar{\text{d}}) &= \text{V}_{\text{on}_\text{t}} < \text{I} >_{\text{T}_4(\bar{\text{d}})} + \text{R}_{\text{on}_\text{t}} \left(\text{I}^{\text{RMS}}_{\text{T}_4(\bar{\text{d}})}\right)^2 \\
&+ \text{V}_{\text{on}_\text{t}} < \text{I} >_{\text{T}_{10}(\bar{\text{d}})} + \text{R}_{\text{on}_\text{t}} \left(\text{I}^{\text{RMS}}_{\text{T}_{10}(\bar{\text{d}})}\right)^2 \\
&= 2 \times \left[\text{V}_{\text{on}_\text{t}} < \text{I} >_{\text{T}(\bar{\text{d}})} + \text{R}_{\text{on}_\text{t}} \left(\text{I}^{\text{RMS}}_{\text{T}(\bar{\text{d}})}\right)^2\right]
\end{aligned}$$

Therefore, the total conduction losses for the semi–soft switching topology is:

$$\begin{aligned}\mathrm{Total_{SmeiS}} = 3 \times \{&\mathrm{CondLoss_{D_1+D_7}(d) + CondLoss_{T_1+T_7}(d)} \\ &\mathrm{CondLoss_{D_4+D_{10}}(\bar{d}) + CondLoss_{T_4+T_{10}}(\bar{d})}\}\end{aligned}$$

where,

- $\mathrm{V_{on_d}}, \mathrm{R_{on_d}}, \mathrm{V_{on_t}}$ and $\mathrm{R_{on_t}}$ are available on the manufacturer's datasheets.
- d is the duty cycle.
- $\bar{\mathrm{d}} = 1 - \mathrm{d}$.

Table 5.2: Average and RMS currents for the semi–soft switching topology

Topology	**Device**	**Current**	**Formula**
Semi–Soft Switching	Diode	$\mathrm{I_{ave}}$	$\frac{\hat{V_{\mathrm{out}}}}{2\pi\lvert Z_{\mathrm{Load}}\rvert}\left[\frac{sin(\frac{\pi}{6}-\frac{\pi}{n})\times sin(\frac{2\pi d}{n})}{sin(\frac{\pi}{n})}\right]$
	Diode	$\mathrm{I_{rms}}$	$\frac{\hat{V_{\mathrm{out}}}}{\lvert Z_{\mathrm{Load}}\rvert}\left[\frac{d}{6}+\frac{d}{n}-\frac{1}{8\pi}\frac{sin(\frac{\pi}{3}+\frac{2\pi}{n})\times sin(\frac{4\pi d}{n})}{sin(\frac{2\pi}{n})}\right]^{1/2}$
	Transistor	$\mathrm{I_{ave}}$	$\frac{\hat{V_{\mathrm{out}}}}{2\pi\lvert Z_{\mathrm{Load}}\rvert}\left[\frac{sin(\frac{2\pi d}{n})\times sin(\frac{\pi}{6}+\frac{\pi}{n})}{sin(\frac{\pi}{n})}\right]$
	Transistor	$\mathrm{I_{rms}}$	$\frac{\hat{V_{\mathrm{out}}}}{\lvert Z_{\mathrm{Load}}\rvert}\left[\frac{d}{12}+\frac{d}{2n}+\frac{1}{8\pi}\frac{sin(\frac{\pi}{3}+\frac{2\pi}{n})\times sin(\frac{4\pi d}{n})}{sin(\frac{2\pi}{n})}\right]^{1/2}$

Therefore,

$$\begin{aligned}\mathrm{P_C} = &3 \times (\mathrm{V_{on_d}} + \mathrm{V_{on_t}})\frac{\hat{V_{\mathrm{out}}}}{\pi\,\lvert Z_{\mathrm{Load}}\rvert}cos(\frac{\pi}{n})cos(\frac{\pi}{n}(2d-1))+ \\ &3 \times (\mathrm{R_{on_d}} + \mathrm{R_{on_t}})\left(\frac{\hat{V_{\mathrm{out}}}}{\lvert Z_{\mathrm{Load}}\rvert}\right)^2\left[\frac{1}{4}+\frac{1}{2n}-\frac{1}{4\pi}sin(\frac{2\pi}{n})cos(\frac{2\pi}{2}(2d-1))\right] \quad (5.8)\end{aligned}$$

5.3 Switching Process

5.3.1 Hard Switching

Fig. 5.2 shows the switching signals for the hard switching topology and the dead–time. It can been seen from the figure that all the switches are off during the dead–time and the load current will flow through the snubber circuit causing voltage spikes as shown in Fig. 5.3

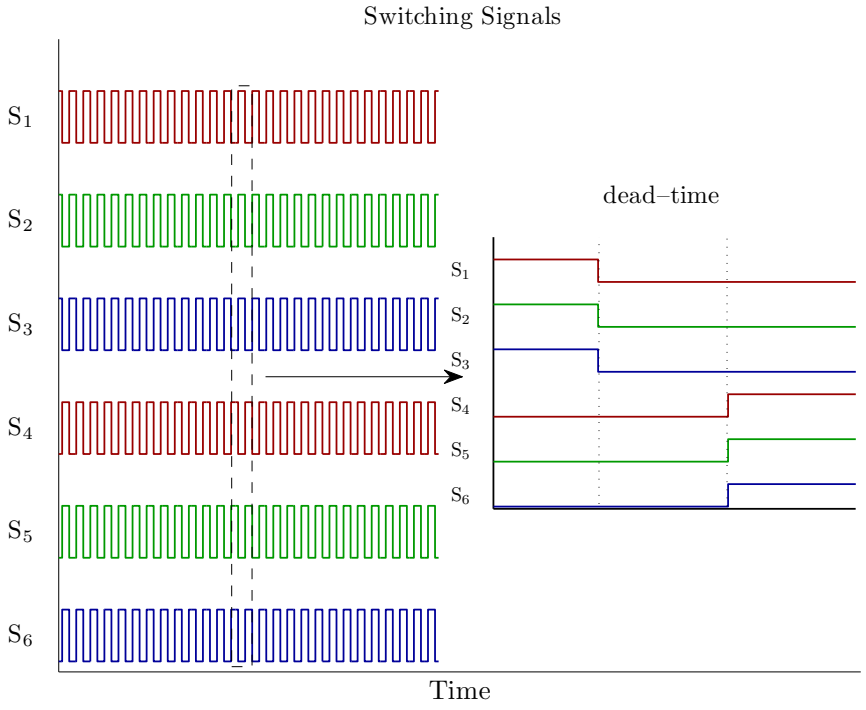
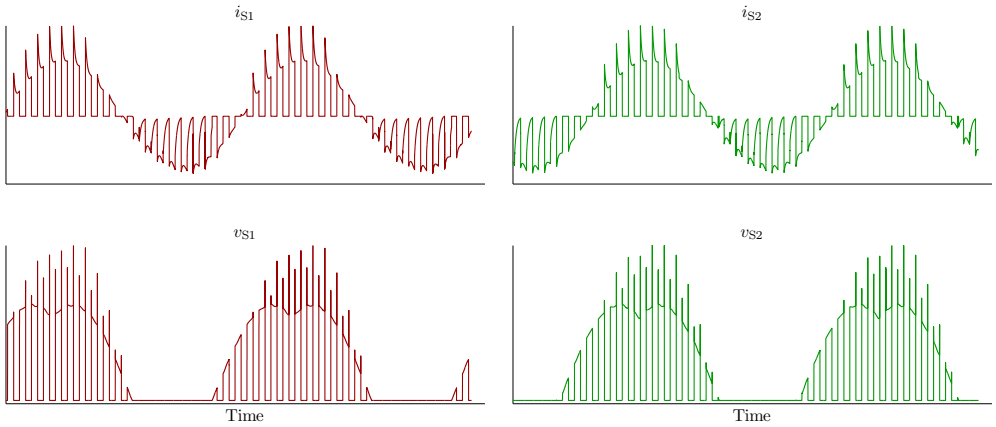


Figure 5.2: Hard Switching Pulses

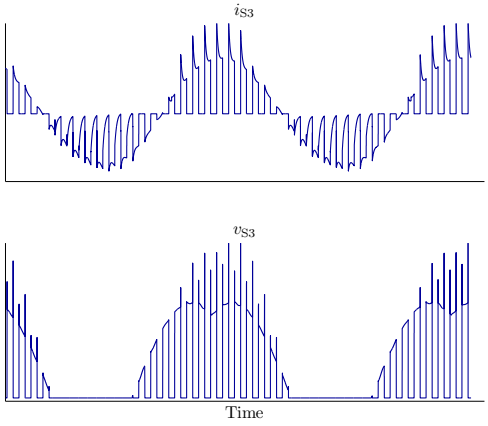
5.3.2 Semi–Soft Switching

Fig. 5.4 shows the switching signals for the semi–soft switching topology with the pulses of the current directions. Although there are twelve switches in



(a) Phase A

(b) Phase B



(c) Phase C

Figure 5.3: Switching Currents and Voltages

the semi–soft switching topology shown in Fig 2.8, there are only three switches which are *on* all the time as can be seen in Fig. 5.5 by zooming in on Fig. 5.4

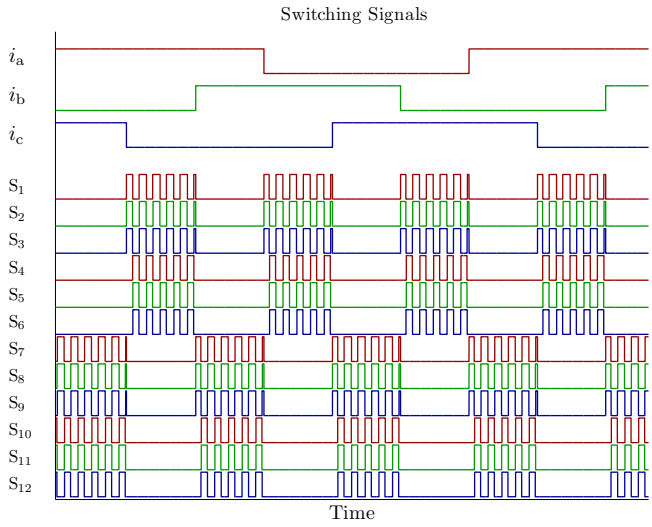


Figure 5.4: Semi–Soft Switching Pulses

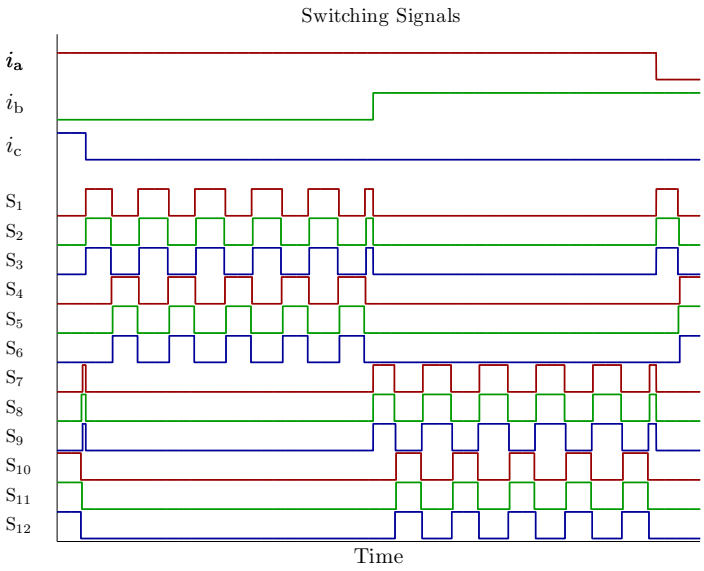


Figure 5.5: Semi–Soft Switching Pulses

5.4 LOSSES AND EFFICIENCY COMPARISON OF BOTH CONVERTERS

A complete list of parameters is presented in Table 5.3 for both topologies.

Table 5.4 shows the result of the analytical calculations compared against matlab simulations. It can be seen that the results from both methods are approximately consistent. During one switching period in the semi–soft switching topology, there is only one switch that has hard switching and the other switches have soft switching. In general, all the switches that connect the load to the source have hard switching as shown in Fig. 5.6. However, the other six switches have soft switching all the time as shown in Fig. 5.7. Consequently, the switch-

Table 5.3: Prototype Parameters

System Parameters	
Mains	$V_{\text{in}} = 208(\text{V})$, $F_{\text{p}} = 60(\text{Hz})$
Isolation transformer	$n = 1:1$
Load	$R = 100(\Omega)$, $L = 100(\text{mH})$, $S_{\text{L}} = 405(\text{VA})$
Hard Switching Converter Parameters	
MOSFETs	FDD6N50 , $V_{\text{DS}} = 500(\text{V})$, $I_{\text{D}} = 6(\text{A})$
Snubber Circuit	$R_{\text{s}} = 700(\Omega)$, $C_{\text{s}} = 0.2(\mu F)$
Duty Cycle	50%
Switching frequency	1.2(kHz)
Dead–Time	$2(\mu sec)$
Semi–Soft Switching Converter Parameters	
MOSFETs	FDP5N50F , $V_{\text{DS}} = 500(\text{V})$, $I_{\text{D}} = 4(\text{A})$
Switching frequency	1.2(kHz)
Duty Cycle	50%

ing losses are distributed in the six switches beside the voltage source, while the other six switches have no switching losses at all.

Table 5.4: Loss Calculation

	Hard Switching	
	Analytical Solution	Computer Simulation
Switching Losses	4.9 (W)	4.61 (W)
Conduction Losses	3.26 (W)	3.27 (W)
	Semi–Soft Switching	
	Analytical Solution	Computer Simulation
Switching Losses	2.72 (W)	2.46 (W)
Conduction Losses	3.26 (W)	3.24 (W)

The main advantage of hard switching is that there is no need to measure the load current, while the disadvantage is the design of the snubber circuit which is necessary to do hard switching. However, the main disadvantage of semi–soft switching is the need to know the current direction. Also, measuring devices are expensive in high power applications. In general, semi–soft switching is more efficient than hard switching as shown in Fig. 5.9(a), and the switch in semi–soft switching topology overcame the AC choppers switching problems without increasing the conduction losses as shown in Fig. 5.8(a) and Fig. 5.8(b).

5.5 Semiconductors Ratings

Power semiconductor of the device can be specified by the maximum voltage the device can block and the average current the device conducts. The analytical

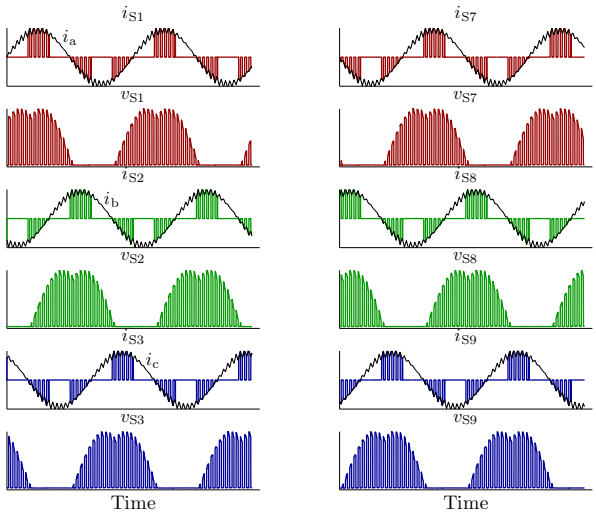


Figure 5.6: The Switches with Hard Switching

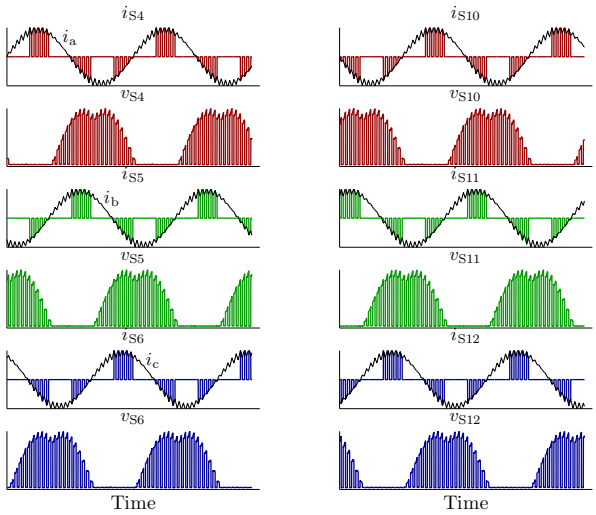
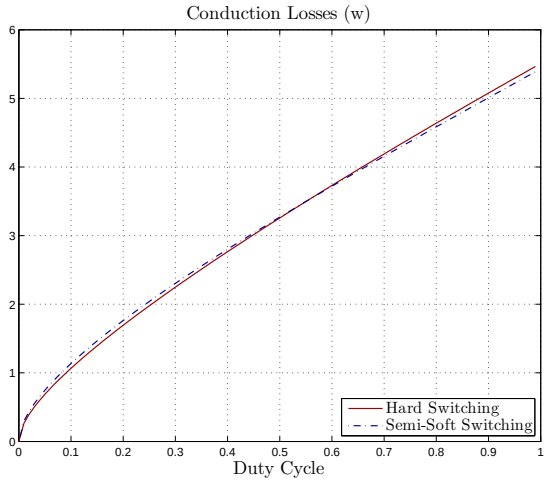
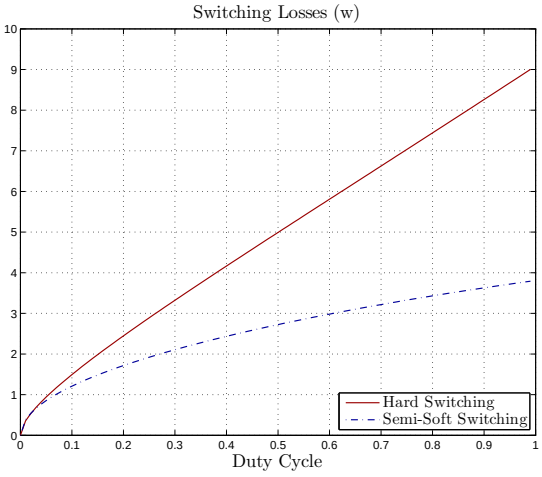


Figure 5.7: The Switches with Soft Switching



(a) Conduction Losses



(b) Switching Losses

Figure 5.8: Conduction and Switching Losses

formulas that express the ratings can be developed as follows:

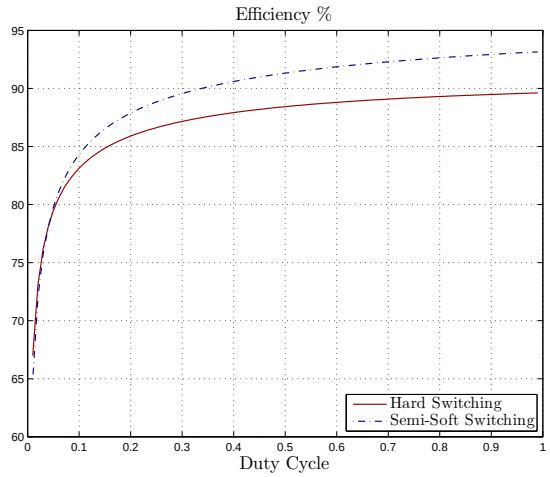
5.5.1 Hard Switching

$$\begin{aligned} \mathrm{S_i(VA)} &= 3 \times V_{\mathrm{off}} \left\{ < \mathrm{I} >_{\mathrm{T_1(d)}} + < \mathrm{I} >_{\mathrm{D_1(d)}} + < \mathrm{I} >_{\mathrm{T_4(\bar{d})}} + < \mathrm{I} >_{\mathrm{D_4(\bar{d})}} \right\} \\ &= 3 \times V_{\mathrm{off}} \frac{\hat{V_{\mathrm{out}}}}{2\pi |Z_{\mathrm{Load}}|} \left[4cos(\frac{\pi}{n}) cos(\frac{\pi}{n}(2d-1)) \right] \end{aligned}$$

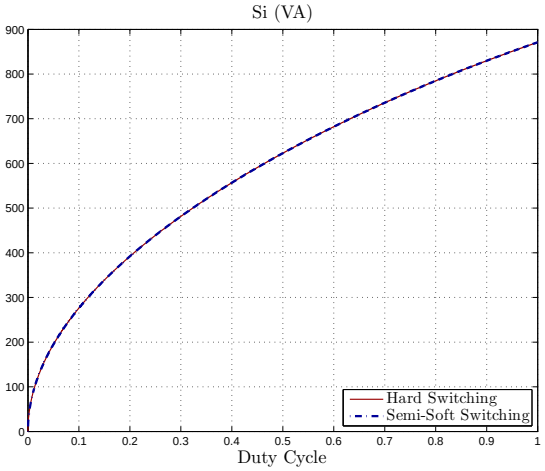
5.5.2 Semi–soft Switching

$$\begin{aligned} \mathrm{S_i(VA)} &= 3 \times V_{\mathrm{off}} \{ < \mathrm{I} >_{\mathrm{T_1(d)}} + < \mathrm{I} >_{\mathrm{D_1(d)}} + < \mathrm{I} >_{\mathrm{T_7(d}} + < \mathrm{I} >_{\mathrm{D_7(d)}} \\ &\qquad + < \mathrm{I} >_{\mathrm{T_4(\bar{d})}} + < \mathrm{I} >_{\mathrm{D_4(\bar{d})}} + < \mathrm{I} >_{\mathrm{T_{10}(\bar{d})}} + < \mathrm{I} >_{\mathrm{D_{10}(\bar{d})}} \} \\ &= 3 \times V_{\mathrm{off}} \frac{\hat{V_{\mathrm{out}}}}{2\pi |Z_{\mathrm{Load}}|} \left[4cos(\frac{\pi}{n}) cos(\frac{\pi}{n}(2d-1)) \right] \end{aligned}$$

Although the number of the devices has been increased in the semi–soft switching, the total semiconductor (VA) for both topologies is the same as shown in Fig. 5.9(b).



(a) Efficiency



(b) Power Semiconductor

Figure 5.9: Efficiency and Power Semiconductor

5.6 Conclusion and Future Work

5.6.1 Conclusion

There are various topologies for implementing an AC chopper in distribution systems, as well as in transmission systems. Therefore, the semi–soft switching topology can be used in applications such as voltage control at sensitive loads, voltage sag compensators in the distribution system, and power flow control transmission power systems.

For reducing turn–on and turn–off losses in the power switching devices, the semi-soft switching topology shows better efficiency than the hard switching topology. All the formulas in both topologies may be used for estimating losses and in the design of such converters. Finally, after considering the effects of dead time in the hard switching topology, the result deviates from the ideal one.

Although the number of switches in the semi–soft switching topology was increased, the total of conduction losses did not increase.

5.6.2 Future Work

The work in this research may be extended to experimental implementation in the lab, in order to compare the simulation results with the experimental results. Also, a closed loop controller may be designed to deal with unbalanced issues by changing the duty cycle.

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